HETEROGENEITY ON SILICON OR IN A PACKAGE FOR FUTURE SYSTEM INNOVATION

EXECUTIVE SUMMARY

In the coming decade silicon devices will be divided into two main categories:

(1) bit rate performance driven digital ICs, following Moore's law on the ITRS roadmap, for which the US area is dominant,

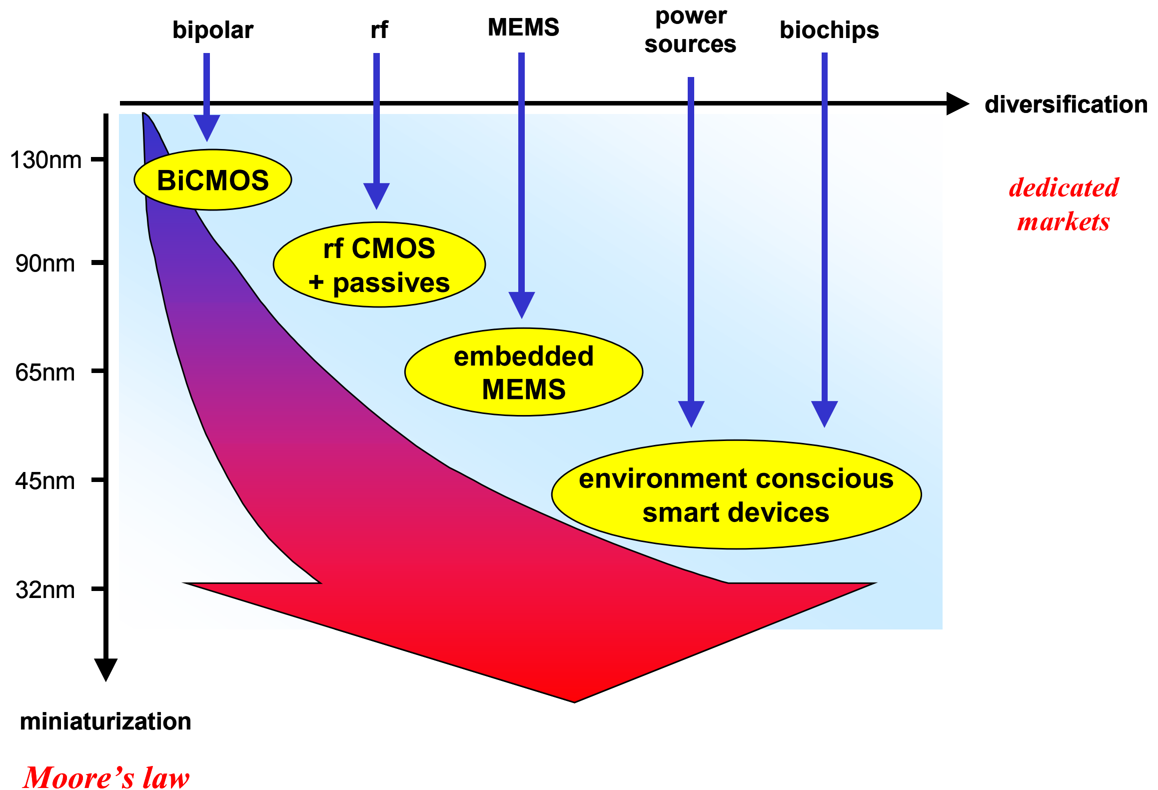
and

(2) mixed signal heterogeneous devices driven by cost and also other requirements such as low energy dissipation and integration of various technologies, where Europe may have a strong leadership. This category of devices follows a more diversified roadmap where the minimal dimension of the transistor is only one of the key parameters of the technology along with mixed-mode or RF components, embedded MEMS and bio-functions.

For this type of system, **heterogeneity on silicon or in a package** is the main feature for system integration.

Due to the growing importance of heterogeneous systems for the European semiconductor industry, a subcommittee of the MEDEA+ Scientific Committee was formed, with experts from CEA-LETI, Fraunhofer Gesellschaft (FhG) and IMEC. A contribution from industrial experts was added at a later stage.

For the sake of simplicity, the report focuses on silicon technologies*, excluding optical devices and systems, as well as flexible electronics (e.g. on plastics)*. In the same way, harsh environments requiring dedicated technologies are not specifically discussed. It should also be stressed that embedded software is not detailed in the document, though it contributes to a large extent to the final cost of the system.



Many important applications for heterogeneous systems fit in the 'Ambient Intelligence' theme, where integrated systems are defined as smart devices which are conscious of and self-adapting to their environment while communicating with a dynamically reconfigurable network of other devices. Technological challenges include extremely low-leakage CMOS, high quality RF devices (passives, MEMS, etc.) and new packaging solutions. The major design challenge deals with the co-design of programmable and reconfigurable multiprocessor architectures with distributed memories and including embedded software, broadband radios, etc.

For the longer term, completely three-dimensional packaging solutions of chips coming from extremely heterogeneous technologies must be developed as sketched by the "e-grain" or "smart dust" concepts. Here, novel power sources based on thin film batteries, fuel cells, inductive coupling or various MEMS concepts must be considered, as well as sophisticated physical and (bio)chemical interfaces to and from the outside world. The ability to exchange a broad range of complex design parameters between devices from different technologies, packages, and systems in a concurrent co-design targeted towards lower cost will be an extraordinary challenge, needing to close additional technical and cultural gaps through a multidisciplinary approach.

The major technology directions are covered in the document along two broad routes, namely the system design side, with a specific discussion on test, and the system packaging technology, with key focus on the wafer level packaging, the vertical integration and the System-in-a-Package concept, adding a separate discussion on the integrated energy supply.

The report is intended to be neither a roadmap nor a market study, but rather aims at describing various scenarios for the next decade in the field of heterogeneous systems on silicon or in a package including an analysis of the strengths and weaknesses in Europe.

The major findings of the study are listed below:

-A holistic approach to the design of systems that have a high degree of heterogeneity should be promoted. This requires a new collaborative and multi-disciplinary approach to system level design and technology research driven by well-chosen long term focused application domains. Testing of heterogeneous systems in particular requires R&D efforts.

-There is a need for advanced research in design methodologies for mixed signal, RF design, ultra-low power multiprocessor architectures.

-Major breakthroughs are needed in a multi-scale co-design of chip and package in order to optimize the overall size, performance and cost of the system. It includes an efficient partitioning between monolithic parts and the package.

-Development of advanced technologies for Systems in a Package are mandatory, e.g. to accommodate the reduced mechanical stability and heat conductivity of new interconnects and the introduction of new materials for RF components, higher density and multi-layer technology on flexible substrates.

-The heterogeneous systems should integrate the power devices and power management in their design flow and fabrication.