Catrene updates European EDA roadmap

By Peter Clarke

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LONDON — Catrene, the pan-European collaborative R&D initiative intended to take electronics into the nanoscale era, has released its 2009 European EDA roadmap. The document is described as a "substantial" update to the 2005 edition of the Medea+ EDA roadmap.

"The global strategic European objective of this new roadmap is to engineer design solutions more rapidly, originating from system users specifications in a top down design flow within various silicon application platforms of choice and to develop early parametrizable and reusable system IPs for the next generation of products," said Enrico Villa, chairman of Catrene.

The roadmap covers top-down design, system-level design, parametrisable IP creation, standards and design for manufacturability (DfM) supported by TCAD (Technology CAD) developments. Furthermore, the roadmap includes basic digital functions such as multiprocessor cores, value-added functionalities such as analog, radio frequency, embedded memories and micro mechanical functions, with more design reusability, a major objective of the program. The roadmap pinpoints specific needs, at particular points in time, and with a specific time frame of 2008 to 2013.

The roadmap was available for downloading from http://www.catrene.org/web/communication/publ_eda.php when this story was first posted.

Catrene is a four-year program which started Jan. 1 2008 and is extenable by a further four years. Catrene is expected to deploy about 4,000 person-years annually, equivalent to about 6 billion euro (about $7.7 billion) for the extended program.