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EDA firms team to improve design for mask manufacturing

Anne-Francoise Pele
EE Times Europe
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PARIS — The 46th Design Automation Conference comes with its fair share of partnership annoucements. Toppan Photomasks France SAS (Corbeil Essonnes, France), Satin IP Technologies SAS (Montpellier, France) and Xyalis Sarl (Grenoble, France) announced they have joined forces to improve design for mask manufacturing (DFMM).

This collaboration falls within a European collaborative R&D program, dubbed Crystal and sponsored by the the Cluster for Application and Technology Research in Europe on NanoElectronics (CATRENE).

A key mission of the Crystal program consists in identifying and formalizing recommended design practices to make mask manufacturing a more efficient and less iterative process. Crystal also aims to provide the tools to deploy and monitor those practices throughout the design chain.

"Designing chips so that photomasks can be manufactured more easily is a complex challenge that cannot be solved without tight collaboration between chip design teams, semiconductor fabs, mask shops and EDA vendors," commented Michel Tissier, European technology integration director at Toppan Photomasks France and head of the Crystal program.

He continued: "By making these different groups work with

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Bonus? Hah! More like rounding error.
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Satin IP's VIP Lane on real manufacturing data, Crystal is expected to help improve design consistency, on-time delivery and the cost of photomask design."

Satin IP launched its VIP Lane in April 2007. This quality management software is said to support design engineers and project managers in their efforts to make design-for-reuse a daily reality.

Complementing and interoperating with EDA and PLM tools, VIP Lane is claimed to work as an implementation channel for design-for-reuse processes which semiconductor companies usually have in place. The solution runs on a web server application and captures all parameters and objects affecting IP quality, from multiple sources throughout the IP design and integration lifecycle, asserted Satin IP.

Michel Tabusse, founder and CEO of Satin IP Technologies, declared: "Crystal will give us access to real data about the manufacturing challenges at mask shops and about the design practices in the upstream design phases that would solve these challenges. We plan to use these data to create an unmatched library of DFMM quality checks as an add-on to VIP Lane."

A design environment prototype, offering a first set of design rules with monitoring capabilities and links to mask data preparation tools, was demonstrated at the Euro Nanoelectronics Forum in Paris in December 2008. An updated prototype will be showcased at DAC in San Francisco, at the end of July.

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