The move to 450mm: Europe's perspective

The European Equipment and Materials 450mm Initiative (EEMI450) provides Europe's perspective on the transition to 450mm wafers

In 2009 the European Semiconductor Equipment and Materials industry decided to form a 450mm dedicated initiative, called EEMI450, to bring the interested parties together, to promote common 450mm efforts and to induce common 450mm European projects. Currently, this Initiative has more than 45 members, and to date, four 450mm European research projects have been labeled through the European ENIAC and CATRENE funding instruments.

The EEMI450 Initiative has written a white paper which defines the goals of the EEMI450 Initiative and in which the economical motivation concerning the 450mmm wafer transition for the semiconductor industry is explained. The white paper emphasizes the importance of early engagement in 450mm research and development activities for the European semiconductor related equipment and materials industry, which plays a significant role in the global semiconductor marketplace. In February, the white paper was delivered to Neelie Kroes, Vice-President of the European Commission and Commissioner for the Digital Agenda. The following is an excerpt from that white paper. The entire white paper can be found online at www.eemi450.net/White_paper_EEMI450_Final.

The semiconductor manufacturing industry has undergone dramatic growth during the second half of the last century, and throughout the first decade of the new millennium. A primary driver of that growth is the realization of "Moore's Law", whereby the number of transistors in an integrated circuit doubles approximately every 2 years with an associated increase in circuit functionality, reduction in operational power, and a reduction in unit cost. This, in turn, leads to an increased market demand for consumer products containing silicon integrated circuits, such as personal computers, mobile phones, and other electronic devices.

From left to right: Bernie Capraro, EU Research Programme Manager, Intel Ireland (co-author of the EEMI450 White Paper); Neelie Kroes, Commissioner for the Digital Agenda and Vice-President of the European Commission; Rob Hartman, Director Strategic Technology Program, ASML (member of the EEMI450 initiative); Bas van Nooten, Director European Cooperative Programs, ASM International (chairman of the EEMI450 initiative); and Heinz Kundert, President, SEMI Europe.

As an economic consequence, the silicon wafers used in the manufacturing processes to produce the silicon chips have undergone a diameter increase approximately every 10 years to improve throughput and reduce manufacturing costs. Silicon wafers that have been used in high volume manufacturing processes range from 1-inch diameter, to the current state-of-the-art diameter of 300mm (11.8- inch, usually referred to as 12-inch). During this wafer size evolution, the ever increasing complexity of the supply chain of semiconductors has, and continues to demand, an increasing involvement from materials suppliers and equipment manufacturers.

Tier 1 initiatives

The next silicon wafer size is destined to be 450mm (18-inch), and activities are currently underway amongst the Tier 1 Semiconductor Manufacturing Companies, Intel, Samsung, TSMC and others, to prepare for manufacturing using this next wafer size in the second half of the current decade. In order for this to happen, a plethora of technological breakthroughs are required from the Equipment and Materials organizations, beyond a simple scale-up and extension of current

technologies. This represents a global challenge as these organizations operate in all regions of the World. The European Equipment and Materials organizations therefore have a key role to play in this activity. By taking this initiative to be involved in this next wafer size transition, they will have the opportunity to establish share of the 450mm equipment and materials market.

Why the transition to the next generation wafer size? There is one fundamental and compelling question to be answered at each of the semiconductor manufacturing industry's wafer transitions; from the very early 2-inch diameter and less generations of the 1950's and 60's, through the 3-inch and 4-inch of the 1970's, the 5-inch and 6-inch of the 80's, the 200mm (8-inch) of the 90's, the 300mm (12-inch) of the 2000's, and now the 450mm (18-inch) generation expected in the second half of this decade and second century of semiconductor manufacturing. That question is: Why is a 50%-diameter increase in semiconductor processing platform needed about every decade?

As with the previous wafer size transitions, the move to 450mm is largely driven by the productivity, environmental, and economic challenges of the semiconductor industry as it continues to evolve. In particular:

• The number of semiconductor manufacturing fabrication facility ("fab") construction projects must be sustainable based on both its manufacturing complexity and environmental impact;

• The productivity and thus the economic feasibility of semiconductor manufacturing costs must be preserved [normalized for analysis purposes as cost per square centimeter (cost/cm^2)] in the face of continuous and exponentially increasing manufacturing facilities, equipment and materials costs. These costs are driven by the technology investments required to meet customer expectations for the doubling of functionality and performance approximately every 2 years, as defined by Moore's Law.

If we look at the data governing the volume of silicon shipped during the history of the semiconductor industry (based upon the SEMI® silicon shipment history), we can see that, historically, the baseline demand compound annual growth rate (CAGR) is a constant 7.6% since 1993, and prior to that was 15%, with periodic cycles around 2inch, 4inch, 6inch and 8inch silicon wafers used in semiconductor manufacturing processes these core rates. These major business cycles have occurred with a 7 to 8-year periodicity, with a minor "slowing" cycle in between the major cycle trough and peak.

Another factor affecting the growth rate of the industry is the overall downward trend of the Average Selling Prices (ASPs), which in effect has turned what used to be luxury electronic devices into commodity goods for the general public.

At a CAGR of 7.6%, the amount of silicon shipped for all types of electronic products such as memory, microprocessors, and other specific logic devices would double in less than 10 years. This would therefore require new factory capacity to sustain such growth. In previous wafer size generations, this has led to the adoption of the next-generation wafer size in order to reduce the number of factories to be built and sustained. Therefore, at some point in the future along this demand curve, despite any future possible industry consolidation, it will become more economical for chip makers to build one 450mm factory rather than two 300mm factories.

When the cycle-based demand growth is applied to the ISMI Industry Economic Model in a scenario without the 450mm wafer generation, the number of 300mm equivalent 35K wafer starts per month (wspm) fab capacity increments rises to above 500 fabs, for all wafer generations, by the middle of this decade, and to above 600 fabs into the next decade. Based on this model, the level of fab capacity in any one wafer generation would rise to a level unprecedented in history, and create untenable challenges for companies required to meet the anticipated customer demand associated with many different products. With further potential industry consolidation, and therefore new factory builds resting with fewer companies, these challenges become even more critical.

Even if the size of an individual company's actual site (versus normalized 35K wspm equivalent increments) grows to take advantage of scale, the pressures upon the company resources for personnel, training, and facility infrastructure will be challenging even under the 300mm-only scenario. In addition, the environmental impact of water usage, sewage effluent, and efficient materials and energy usage will be far greater on a per square centimeter basis, as demonstrated by the 300mm wafer generation's own history during the 200mm to 300mm transition from 2001 -2010.

Another consideration in the absence of 450mm manufacturing would be the number of incremental new 300mm fab additions required to support the growing semiconductor market. This would be greater than the number of 450mm facility builds required, and hence could increase the number of annual build projects above the historic steady and sustainable level.

A 450mm roadmap

Looking from a cost perspective, historically, the cumulative cost per transistor benefit, weighted across all product types (with memory functionality most heavily weighted) resulted in a compound reduction of cost per function of -29% per year. This reduction was a combination of doubling the functionality in a square centimeter every two years (as per "Moore's Law") and keeping the cost of manufacturing for that square centimeter approximately flat. The benefit of a new wafer size generation's productivity has been estimated in the past by "resetting" by a 30% cost reduction every 10 years the ~3-4% /year exponentially increasing costs due to technology cycle upgrades and insertions, e.g., copper interconnects replacing aluminum.

Although not necessarily desired, the ITRS has been anticipating a slowdown in the rate of the technology cycle from 2 years, to 3 years, resulting in a slowing of the functional density in a square centimeter. In the absence of a 450mm productivity solution, the net slowdown effect upon the combination of the slower density and the higher cost per square centimeter results in only a -27% average cost/transistor reduction rate. This may appear to be a minor effect, but over the 2006 – 2024 timeframe, the slower rate produces a cumulative ~1 trillion dollar productivity difference impact without the 450mm wafer generation productivity gain. (In order to arrive at this statement, an in depth analysis should be performed per product type, taking in to account certain industry specific details e.g. EUV introduction, initial high cost of 450mm silicon and Flash cost growth due to 3D layer implementation.

The ability to extend Moore's Law into the future is dependent upon the development and production of new semiconductor manufacturing equipment. The operating costs associated with the silicon IC manufacturing Industry are heavily dominated by the cost of the equipment depreciation and maintenance. Therefore, by providing a new generation of processing equipment for 450mm silicon wafers, IDM, Foundry and OEM organizations are set to benefit in the future, and enable the sustained growth of the Industry.

There exists an outstanding benefit for European Equipment and Materials manufacturers to pool their efforts, to get support by Public Authorities at European and National level on their first steps into this required research and development. Thus, not only the 450mm technology will become a success story, but also the next generation of 300mm equipment and the More-Than-Moore fabs will have strong benefits, resulting presumably in safeguarded employment and in several thousands of new, high quality jobs across Europe. Perhaps to reduce risk, innovations on 300mm equipments and then scale up to 450mm may be a sometimes preferred route for both OEMs and IDMs, and subsequent process technology development on 300mm wafers, then scale up, a cheaper approach for IDMs to follow. The presence of an appropriate supply chain, and of customers of 450mm processed wafers, could be an invaluable attraction to maintain semiconductor production in Europe and to consider Europe for additional 450mm fabs.