EDA autobahn

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CATRENE releases the 2009 European EDA Roadmap

The 2009 European EDA Roadmap is a substantial update of the 2005 edition of the MEDEA+ EDA Roadmap. The whole European EDA excellence and expertise from industry, SMEs, institutes and academia organised by Europe's most prominent cluster for cooperative R&D in nanoelectronics have contributed to the new programme.

Enrico Villa, CATRENE Chairman commented: "The global strategic European objective of this new Roadmap is to engineer design solutions more rapidly, originating from system users specifications in a top down design flow within various silicon application platforms of choice and to develop early parametrisable and reusable system IPs for the next generation of products".

The semiconductor industry has been growing at an unprecedented rate since the early 1960s. It capitalised on the outstanding properties of silicon and its stable oxide, which allowed the advent of the CMOS process, the leading process for the whole semiconductor industry. For more than two decades, a two digit average growth per year in semiconductor sales imposes formidable challenges in terms of huge investments needed for volume manufacturing, complex designs and new research in Electronic Design Automation (EDA) at system level to ensure short time to market and competitiveness.

The new Roadmap focuses on demonstrating a complete top-down design flow, starting at specifications, then System Level Design linking designers to formal customer's specifications, parametrisable IP creation, standards and Design for Manufacturability (DfM) supported by new TCAD (Technology CAD) developments. Furthermore, the Roadmap includes basic digital functions like multiprocessor cores, value-added functionalities such as analogue, radio frequency, embedded memories and micro mechanical functions, with more design reusability, a major objective of the new programme. It addresses specific needs, at particular points in time, and with a specific time frame of 2008 to 2013.

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