Communicating with silicon

Michael Salter explains the main points of the SIAM and Dynamic-ULP projects, both of which utilise advanced silicon technology for emerging high frequency applications

What are the core objectives of the 'Silicon Analogue to Millimetre-wave' (SIAM) technologies project, and what contributions is your research institute, Acreo, making?

The objective was to establish silicon technology platforms for emerging high frequency and mm-wave (mmw) consumer applications, such as 77 GHz automotive radars, 60 GHz wireless networking (WLAN and WPAN) and 100 Gbit/s optical data communications. Acreo's role in the project was to test the feasibility of using 65 nm silicon on insulator (SOI) complementary metal-oxide semiconductor (CMOS) technology for a 100 Gb/s optical transceiver. Using this advanced semiconductor process from STMicroelectronics allowed us to implement a novel transceiver architecture that performed more advanced signal processing functions electrically at microwave frequencies before converting to light for transmission over an optical fibre. This approach allowed more efficient use of the available spectrum; in other words, we were able to transmit more data per bandwidth with our approach.

Alongside SIAM, you are also involved in the Dynamic-ULP project. Do the two link together?

SIAM and Dynamic-ULP are similar projects in that they both advance the state-of-the-art in SOI CMOS process and design technology. Both projects utilise SOI CMOS to make new applications possible and improve the performance of existing applications, such as mobile phone power consumption and battery life, for example. SIAM focused on improving and demonstrating the microwave and millimetre wave frequency performance of the 65 nm SOI process, with applications in higher frequency bands such as microwave optical transceiver and automotive radar. Dynamic-ULP will focus on demonstrating the benefits of the 20 nm SOI process for digital and RF transceiver applications.

Could you discuss the new CMOS for millimetre-wave technologies that SIAM is currently developing with pan-European programme MEDEA+?

The MEDEA+ programme and its successor Catrene exist within the EU Eureka framework and are contributing to maintaining European excellence in advanced CMOS technology. The next generations of shrinking CMOS devices will use silicon-on-insulator (SOI) technology to achieve higher speed, lower noise, lower variability and lower power consumption than the standard (bulk) CMOS technology. This is due to the addition of a very thin layer of silicon-oxide between the silicon substrate and the transistor, which reduces parasitic effects and insulates the devices from the lossy silicon substrate. This results in reduced power consumption and increased speed when comparing the same sized device in a traditional CMOS device.

What advantages are afforded by using SOI technology?

From a CMOS process perspective, SOI technology is the least complicated way to continue Moore's technology scaling law down to and below 20 nm gate lengths. It continues the use of the well-known planar CMOS process, improves the device performance (speed and power consumption) and reduces its variability, while simultaneously reducing the size of the CMOS transistor. SOI devices also have other advantageous characteristics, such as better isolation between transistors, which can lead to less coupling noise between circuit blocks in a wireless transceiver IC. For digital circuits, the advantages of SOI are higher speed, reduced power consumption, better reliability, lower variability in transistor properties, and reduced sensitivity to latch-up.

How are Acreo and its partners combining their efforts to tackle this project? How will you ensure that funding is distributed effectively?

In the Dynamic-ULP project, Acreo, together with ST-Ericsson, will evaluate the 20 nm CMOS SOI process for meeting the requirements of next-generation mobile phone RF transceiver application-specific integrated circuits. Funding for the project in Sweden is provided by Vinnova, the Swedish Governmental Agency for Innovation Systems. Vinnova has specific detailed requirements on joint institute industry-financed research projects regarding funding distribution. Acreo and ST-Ericsson are required to have equally matched resource allocation for the project, which will ensure that the project is closely steered by industrial needs.

Where would you like to focus your research efforts in the future? Are there any other projects that you are currently working on?

In addition to mobile and optical transceivers, we plan to evaluate the use of advanced SOI technology for other applications such as terahertz, optical and RF microelectromechanical systems (MEMS), sensors and power electronics. Acreo has much experience in these areas and is leading many projects involving novel sensor and power device development. The whole area of sensors and sensor systems is growing quickly and the SOI platform is rapidly advancing its capabilities here.

Sizable advances

The cutting-edge **SIAM** technologies project has not only brought the best out of Acreo's team of expert researchers, but has sparked subsequent research into SOI for wireless transceivers

RECENT ADVANCES IN silicon technology mean that its use in millimetre-wave applications has become more economically viable, challenging its gallium arsenide counterparts, especially for high volume applications. In fact, silicon is now being considered for many high frequency applications, which range from automotive radar systems, through wireless local area networks (WLANs) to optical data communications. The move to silicon in high volumes would mean a reduction in cost, and this can result in a greater application of this technology.

For example, in low-cost automotive radar installations, advanced silicon could lead the way to collision avoidance radars being fitted to every new car sold – even low-end models – which would likely bring about a reduction in road traffic accidents. Furthermore, the technology being explored could mean that video streaming and other high bandwidth applications using devices within the home will become wholly possible.

TEEMING WITH POTENTIAL

The technology in question is being developed by the 'Silicon analogue to millimetre-wave' (SIAM) project, and hopes are indeed high that it will make a significant impact upon the telecommunications market. Following the excellent high frequency performance of the consortium's 65 nm silicon on insulator (SOI) complementary metal oxide semiconductor (CMOS) technology, the group has also been able to design an integrated microwave optical transceiver for telecommunications devices. In order to handle the deluge of Internet data traffic, they have been investigating a transceiver architecture called subcarrier multiplexing, which benefits from increased spectral efficiency over traditional approaches. This technique takes the approach of dividing the data into several parallel streams and then performing higher order data modulation in the microwave domain. In comparison to traditional optical transceivers, this technology is able to shift more of the signal data processing from the optical to the electrical domain which, in turn, places a high burden on the silicon process used to implement the integrated transceiver. In this challenging environment, the 65 nm SOI process was demonstrably capable of meeting the high demands of the application.

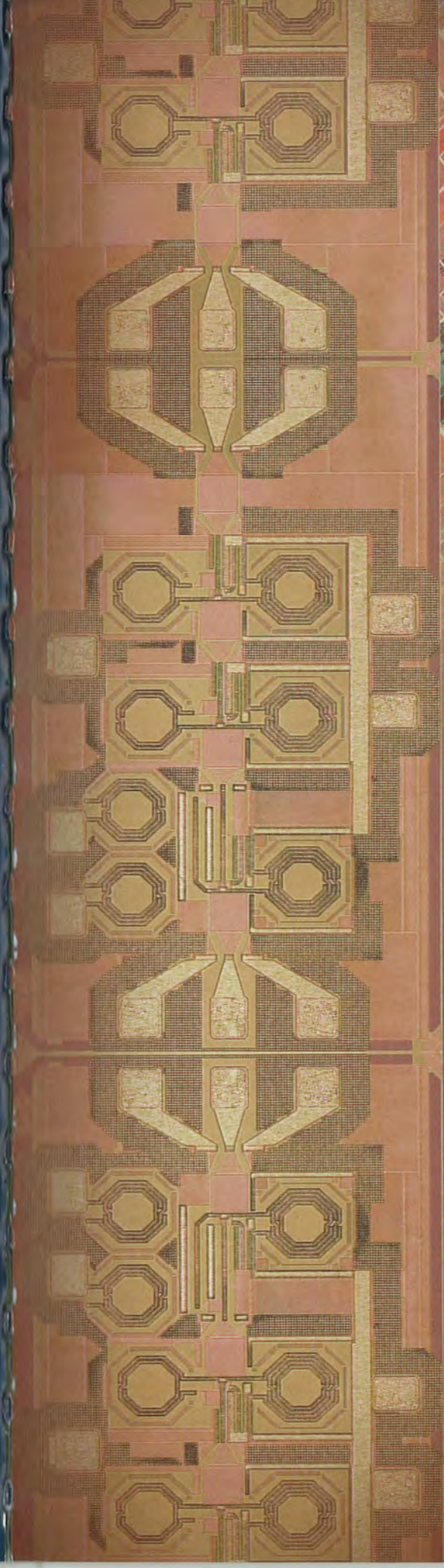
In addition to developing the 65 nm SOI CMOS technology, the project has developed a 130 nm silicon-germanium-carbon (SiGeC) bipolar CMOS. Both are now ready for production, and are capable of performance in excess of 100 Gbit/s for ethernet applications and 77 GHz for automotive radar sensors. The 65 nm SOI CMOS technology has been readied for production and has been demonstrated as a feasible option for high frequency applications at 60 GHz, with key building blocks which addressed the range from 60-94 GHz. These developments open up huge potential for silicon to enter emerging and cutting-edge markets. The ultimate goal for SIAM is to lay the foundations to establish a leadership position for European chipmakers, and the success of the project is the first stage in realising this target.

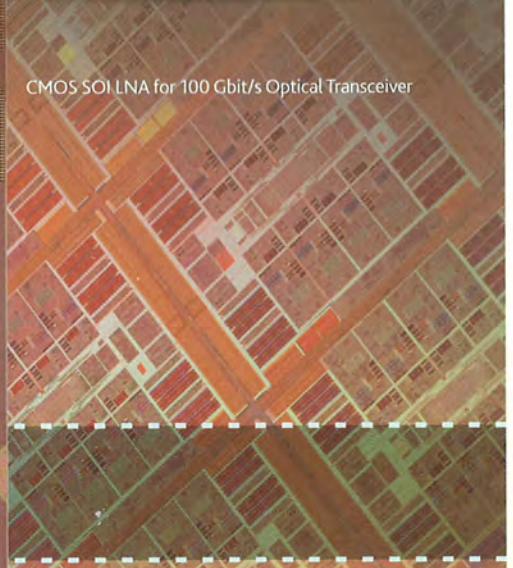
PROGRESSING DYNAMICALLY

Work now continues with the Dynamic ultra low power (Dynamic-ULP) project. This project extrapolates SOI and CMOS development through the scientific committee of the Cluster for the Application and Technology Research in Europe on Nanoelectronics (CATRENE). Once again the project is advancing state-of-the-art SOI CMOS technology by further reducing the transistor size in order to gain benefits. Within the Dynamic- ULP project, the aim is to develop a fully depleted SOI process at the 22/20 nm gate length node. By shrinking the critical dimension down to 20 nm, the transistor channel is entirely depleted of charge carriers, making for a far more consistent transistor with less parameter variation. Additionally, there is the ability for a dynamic trade-off between power and speed, facilitated by the threshold voltage tuning capability of the SOI process. The Dynamic-ULP project hopes that it will be able to utilise this feature for mobile terminals. The chief goal is to develop the 20 nm SOI process technology, as well as the associated design methodologies and tools, and to demonstrate the capabilities for the mobile wireless technology. Pursuing this goal will help to cement Acreo's position at the forefront of the technological improvement of wireless technologies.

A CONFLUENCE OF EXCELLENCE

Heading up these projects at Acreo is Michael Salter who, with over 24 years of engineering and management experience at Motorola and Ericsson, as well as Bachelors and Masters degrees in Engineering from the University of New Hampshire, USA, is incredibly well-positioned to produce technology which is useful to the mobile market. The project includes





CMOS SOI LNA for 100 Gbit/s Optical Transceiver

a wide cross-section of leading industry and academic partners. For Dynamic-ULP, these include nine companies, two research institutes and a university, and the countries of origin range geographically from France to Turkey. Particularly important is the involvement of the world-leading semiconductor manufacturer ST-Microelectronics, who are responsible for developing the silicon platforms based on SOI technology. Other partners have focused on applications. Philips have produced a three-channel 60 GHz beam- forming transmitter with a programmable true time delay matrix, a 60 GHz voltage-controlled oscillator and a 60GHz phase-locked loop, all using the platform developed in SIAM. Similarly, Catena, another partner, developed receiver front-end blocks for the 60 GHz band, which included the low-noise amplifier, voltage controlled oscillator, mixer and quadrature divider.

The ultimate goal for SIAM and Dynamic-ULP is to lay the foundations to establish a leadership position for European chipmakers, and the success of the projects is the first stage in realising this target

Orchestrating the two projects in Sweden, Acreo itself is one of Europe's leading research institutes, and focuses on investigations into electronics, optics and communication technologies. Placed at the juncture between academic research and industry, Acreo aims to produce research which provides practical solutions to problems which can subsequently be marketed and exploited by industry. In the SIAM project, this has been achieved, with results that point to superb performance for commercial applications within the optical communications industry. It is hoped that the Dynamic-ULP project will pick up where SIAM left off, providing exciting solutions to the issues being faced in the wireless communications industry.

INTELLIGENCE

SIAM/DYNAMIC-ULP

OBJECTIVES

SIAM aims at the establishment of silicon technology platforms for emerging high frequency and mm-wave consumer applications, such as 77 GHz automotive radar systems, 60 GHz wireless networking and 100 Gbit/s optical data communication systems.

Dynamic-ULP is focused on setting up a Swedish design platform for complex next generation CMOS system-on-chip design. The design environment will be used to develop circuits and design methods to support ST-Ericsson for their future mobile chipset platforms based on SOI CMOS semiconductor processes.

PARTNERS

SIAM: **Acreo, STMicroelectronics, IMS, Philips, Catena, TU Delft, CEA-LETI, IEMN, Ericsson, SP Devices**

Dynamic-ULP: **Acreo, ST-Ericsson, ST Microelectronics, Ericsson Microelectronic, SOITEC, Atrenta, Infiniscale, Dolphin, CEA-LETI, Catholic University of Louvain**

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MICHAEL SALTER'S research career in telecommunications began at Ericsson, where he focused on analogue and mixed mode simulation for telecom switching infrastructure. In 2002 he joined the Swedish Research Institute, Acreo, where he leads the NanoSystems group performing research and development in silicon-based nanosystems for wireless and sensor applications. His experience has readied him for the challenge of leading both the SIAM and the Dynamic-ULP projects at Acreo.

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