Microsoft and Woking-based McLaren Electronic Systems (MES) have been selected as the official suppliers of electronic control units (ECUs) to the FIA Formula One World Championship for three years, from 2008 to 2010.

The systems will be developed jointly and then manufactured by MES and supplied to all competing Formula One teams for installation on their cars. The ECUs will monitor all aspects of the power train and gather data from over 100 sensors located on the vehicle. Each car's ECU can potentially gather over 1GB of information during a Grand Prix race from the sensors, at an average rate of between 100kB and 500kB of data per second.

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Fujitsu has developed a new bio-based polymer from castor oil. The polymer will be used for small components of notebook PCs and mobile phones, such as connector covers for example, as the new bio-based polymer features superior flexibility and withstands repeated bending.

Fujitsu started using bio-based polymers in 2002, made from materials including corn in the chassis of the FMV-BIBLO notebook PC. However, in order for plant-based materials to be used more widely, what has been needed is a polymer with a higher bio-content that features superior flexibility and is suitable for mass-production.

* * *

Researchers at Infineon have tested the world's first complex circuit fabricated using a new 65nm multi-gate field effect transistor architecture. With an approximately 30% smaller footprint compared to current single-gate technology with the same functions and performance, the new transistors had quiescent current that measured a factor of 10 and less. This will increase the energy efficiency and battery life of portable devices up to two times compared to the 65nm technology going into production today. For future technology nodes (32nm and beyond), this figure will increase significantly.

SOI plus strained silicon will improve device performance

A pan-European collaborative project will create an industrial source of large diameter strained silicon-on-insulator (sSOI) wafers for producing high performance devices.

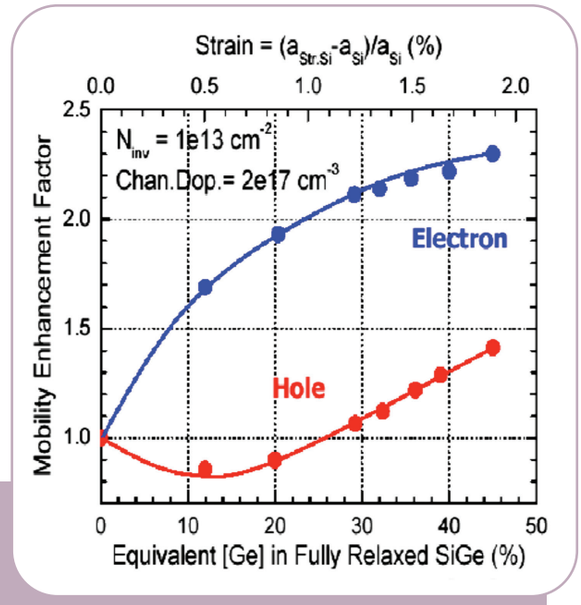
The MEDEA+ project, known as SilOnIS, aims to combine SOI architectures with advanced forms of strained silicon to produce transistors and ICs with improved performance by virtue of the greater charge carrier mobilities and better transistor I_{on}/I_{off} ratios among others. SilOnIS will not only combine SOI with high mobility global strained silicon, but will also use local or 'process-induced' strain at the device level. It is expected to anticipate the requirements of advanced SOI substrates for the next generation of devices using the nodes of 45nm and below.

Project leader Bruno Ghyselen of Soitec, France, explained that as the device dimensions shrink, the transistor scaling calls for more strain in the silicon, yet there is less space for external stressors to be used to create that strain. He said that current results include the demonstration and sampling of 300mm sSOI wafer substrates, including thin fully-depleted (FD SOI) wafers, thick partly-depleted (PD SOI) wafers and FINFET 3D structures.

The researchers have achieved significant sSOI material improvements, with a typical defect density of only 0.2 defects/cm^2. FD SOI devices with 25nm short, narrow gates and a Ti nitride/Hafnium oxide gate stack have been produced.

The partners involved in SilOnIs include Si-based substrate suppliers (Soitec and Siltronic), IC manufacturers (STMicroelectronics, Freescale Semiconductor, NXP), equipment suppliers (ASM and AIXIRON), specific metrology equipment suppliers (Horiba, Sopra, OMI, Accent) and public R&D labs with specialist material expertise (CEA-LETI, MPI Mikrostrukturphysik, Forschungszentrum Jülich).

The project is due to complete in December.



THE PHYSICS BEHIND STRAINED SEMICONDUCTORS

Global strain across a whole wafer level can be attained by the epitaxial growth of silicon onto a layer of relaxed silicon doped germanium (SiGe). Strain occurs because the atomic spacing is slightly larger in SiGe than in relaxed silicon and this stretches the inter-atomic separation of the silicon atoms so that it is similar to that in the SiGe layer.

As the germanium content of the SiGe rises, the strain in the silicon increases and this enhances electron mobility. The amount of strain required to achieve high enhancement of the hole mobility is considerably larger than that needed to similarly enhance the electron mobility.