CATRENE
Programme Review

2015

Cluster for Application and Technology Research in Europe on NanoElectronics

EUREKA Cluster for Application and Technology Research in Europe on NanoElectronics

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EXECUTIVE SUMMARY

CATRENE (Cluster for Application and Technology Research in Europe on Nano-Electronics) is a EUREKA cluster programme dedicated to cooperative research in micro- and nanoelectronics.

The CATRENE cluster programme (E! 4140) was approved by the EUREKA conference in Maribor on 25 October 2007. It was officially announced at the Ministerial Conference in Ljubljana on 6 June 2008, and started on 1 January 2008 as a four year programme to run until year-end 2011. It has since been extended until the end of 2015. In addition to the ongoing activities with respect to cooperative R&D projects, the last two years of CATRENE have been dedicated to a careful assessment of the programme in operation, and to possible improvements.

The following states involved in EUREKA actively support CATRENE: Austria, Belgium, France, Finland, Germany, Ireland, Israel, Spain, Sweden, the Netherlands and Turkey.

This CATRENE Programme Review of 2015 will cover the progress and actions undertaken throughout the year to meet the programme's objective: to foster technological leadership for a competitive European ICT.

Chapter 1 provides an overview of the CATRENE programme while chapter 2 and 3 focus more specifically on 2015 projects and actions.

Overview of CATRENE

The CATRENE programme opened its 1st Call for Project Proposals on 29 February 2008. Today, a total of eight calls have been launched resulting in 52 projects completed, running or about to start, for a total effort of 9142 person-years (PYs). These include 29 CATRENE projects successfully completed by the end of 2015.

Results of CATRENE Call 8

In 2015, CATRENE launched its 8th Call for Project Proposals. Altogether, three projects were labelled, amounting to 571 person-years (PYs).

European Nanoelectronics Forum 2015

The eighth edition of the European Nanoelectronics Forum took place in Berlin, Germany, 1-2 December 2015, and had "Driving Digital Economy" as its theme.

Jointly organised by AENEAS, the EUREKA cluster CATRENE, the ECSEL Joint Undertaking, and the European Commission, the event was well attended, with over 280 participants from all over Europe.

Project NewP@ss (which delivers advanced, secure platforms suitable for the forthcoming third and fourth generation of e-Passport) received the 2015 CATRENE Innovation Award at the Forum. These next generations of e-Passport could be used as certified travel documents within Europe and internationally, and also deployed for hosting dedicated e-services applications (boarding pass support, airline services, and the like) for both, government and private organisations. The world's fastest electronic passport and corresponding reading equipment, which were demonstrated in the context of this project, will improve a traveller's experience, thanks to a faster and automated border crossing procedure. Equally important, the project focused on security and privacy aspects, with the development of new cryptography protocols.

Feedback received in the questionnaire sent to participants at the end of the event showed a high level of satisfaction, particularly with the Project Village and the opportunity it offered to meet and network with people.

1 Overview of CATRENE

The CATRENE programme opened its 1st Call for Project Proposals on 29 February 2008. Today, a total of eight calls have been launched, resulting in 69 labelled projects. By the end of 2015, 29 CATRENE projects had been completed successfully.

CALL	PO received	FP received	Labelled	STATUS OF LABELLED PROJECTS: Cancelled /merged / transferred / suspended	STATUS OF LABELLED PROJECTS: Successfully ended	STATUS OF LABELLED PROJECTS: Active
1ST CALL	**18**	**15**	**14**	**5**	**9**	**0**
Applications	10	8	8	3	5	0
Technologies	8	7	6	2	4	0
2ND CALL	**14**	**10**	**10**	**3**	**7**	**0**
Applications	9	7	7	3	4	0
Technologies	5	3	3	0	3	0
3RD CALL	**15**	**10**	**10**	**3**	**7**	**0**
Applications	7	4	4	2	2	0
Technologies	8	6	6	1	5	0
4TH CALL	**19**	**14**	**10**	**1**	**6**	**3**
Applications	10	8	7	1	5	1
Technologies	9	6	3	0	1	2
5TH CALL	**8**	**5**	**5**	**1**	**0**	**4**
Applications	5	3	3	0	0	3
Technologies	3	2	2	1	0	1
6TH CALL	**13**	**10**	**9**	**3**	**0**	**6**
Applications	9	7	6	2	0	4
Technologies	4	3	3	1	0	2
7TH CALL	**9**	**9**	**8**	**1**	**0**	**7***
Applications	5	5	4	1	0	3
Technologies	4	4	4	0	0	4
8TH CALL	**9**	**4**	**3**	**0**	**0**	**3****
Applications	4	3	3	0	0	3
Technologies	5	1	0	0	0	0
Per 2S 2015	**105**	**77**	**69**	**17**	**29**	**23**

* including one project not started yet
** projects not started yet

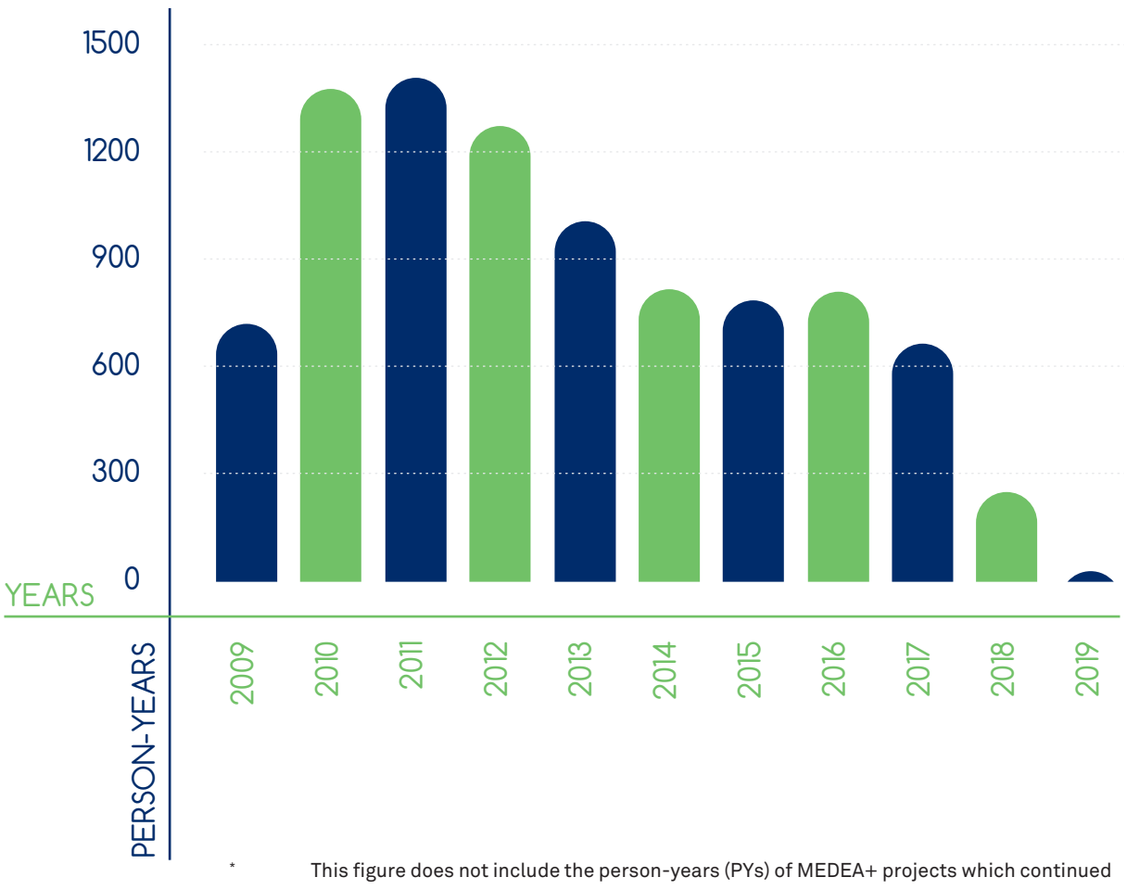
Over the course of the entire CATRENE programme, a total of 17 projects were cancelled/merged due to national eligibility criteria, or funding constraints in some countries (in 2015, a project labelled during the 6th Call was cancelled due to funding issues). The 8th Call was the last call of the CATRENE programme.

Resources, participants and work areas

The following graphs provide an overview of CATRENE project resources (in PYs), project participants and their related work areas.

CATRENE Calls 1 to 8 labelled resources

Total PYs: 9142*

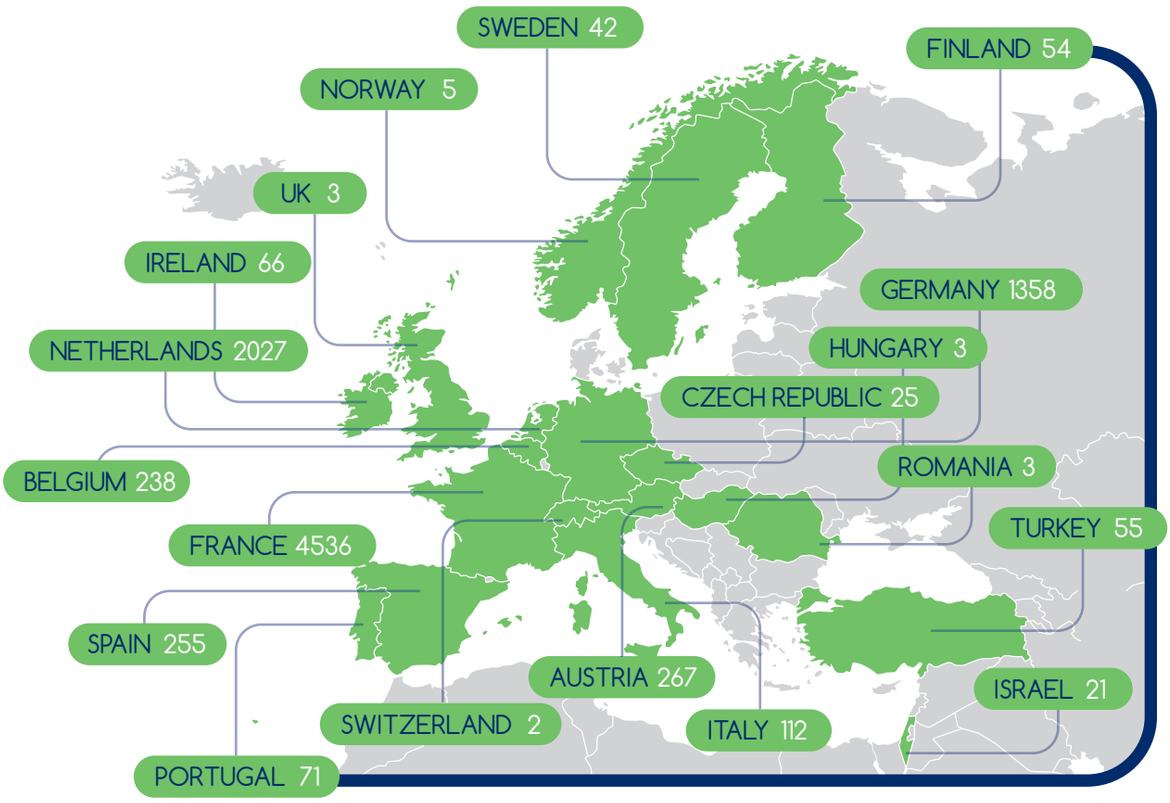


* This figure does not include the person-years (PYs) of MEDEA+ projects which continued running until 2010.

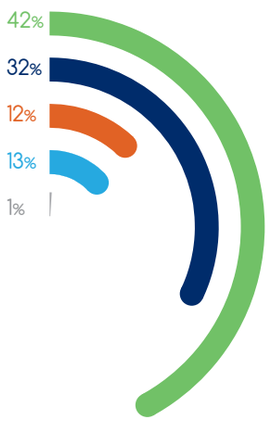
Structure of CATRENE projects

CATRENE Resources per country as per year end 2015

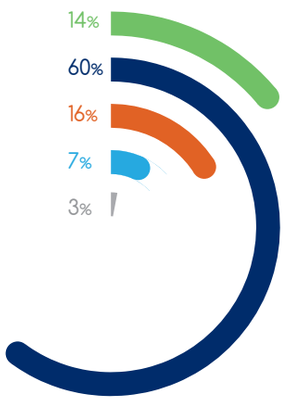
There were 52 projects, 396 participants and 19 participating countries.



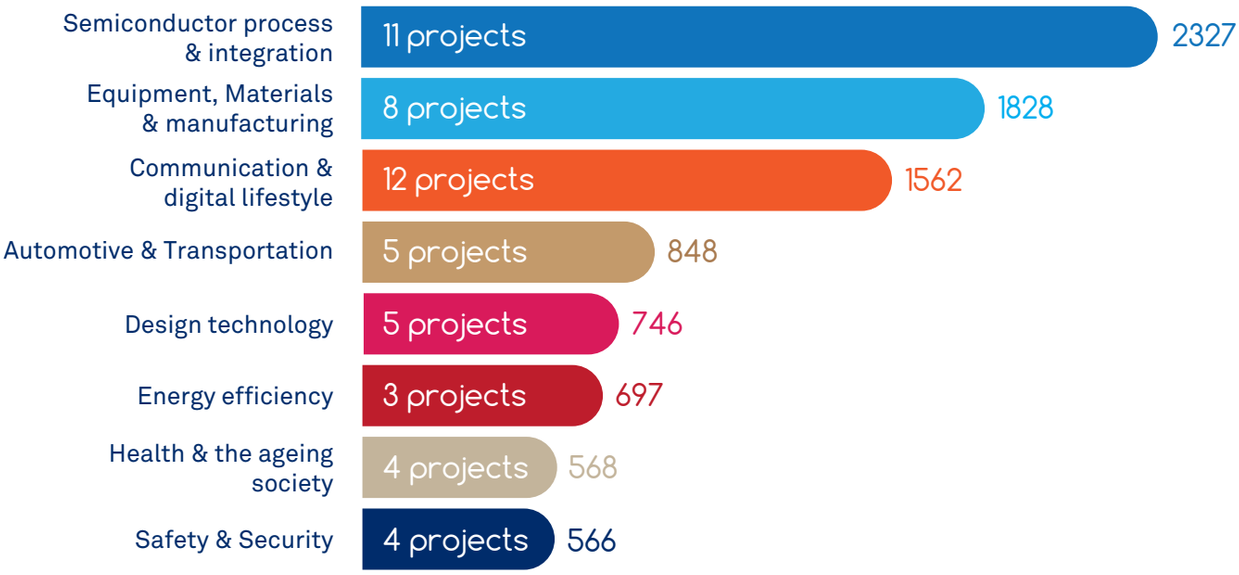
396 participants from 19 countries



Total resources: 9142 PYs



CATRENE labelled projects – split by work area



TOTAL PERSON-YEARS	9142
TOTAL NUMBER PROJECTS	52

For a more detailed list of projects according to work areas, see Appendix B pertaining to the CATRENE projects focus matrix.

2 2015 CATRENE year in review

2.1. Achievements

2.1.1. Call 8

In 2015, CATRENE launched its 8th Call for Project Proposals.

CATRENE Call 8 Now Open

Call opens	18 December 2014	Labelling session
PO submission ends	13 February 2015	01 July 2015
Communication on selected POs	16 March 2015	
FP submission opens	30 March 2015	
FP submission ends	03 June 2015	

Projects start late 2015

Altogether, three projects were labelled by CATRENE as a result of Call 8, amounting to 571 PYs.

More details on the projects labelled in Call 8 are available in Chapter 3 of this publication.

Call			Index	PYs
8	CAT311	Automotive and Transportation [TRACE]	3.1.2	260
8	CAT408	Health and the ageing society [NexGen]	3.1.3	160
8	CAT602	Design technology [PARADISE]	3.1.4	151

2.1.2. Increased links and cooperation with other Clusters / Programmes

CATRENE's mission is to promote and strengthen the European nanoelectronics research, development and innovation (R&D&I) community. This is largely supported by cooperating with other initiatives and organisations linked to the nanoelectronics domain. CATRENE and other EUREKA clusters have been recognised as the only initiatives directly managed by R&D&I actors in regular contact with the EUREKA network and public authorities.

Here are some additional facts about CATRENE:

- CATRENE and its predecessor programmes have existed since 1989, and have continuously collaborated with other EUREKA clusters;
- CATRENE has co-labelled projects with other EUREKA clusters and European-funded programmes like EURIPIDES, ENIAC, ECSEL;
- An Inter-Cluster Committee was created in 2010 to reinforce this cooperation;
- In 2015, CATRENE supported the EUREKA "Smart Cities" initiative by collaborating in a symposium entitled "EUREKA helps French gold nuggets to win Smart City markets", and by issuing a report on "Semiconductors Technologies for Smart Cities";
- To achieve maximum synergy, CATRENE operations are now managed by the industry association, AENEAS, which represents European-based R&D&I actors in micro- and nanoelectronics-enabled components and systems;
- CATRENE organises the annual European Nanoelectronics Forum, in collaboration with AENEAS, ECSEL JU and the European Commission.

2.1.3. Beyond 2015

The CATRENE cluster programme has been evaluating, labelling and monitoring cooperative R&D projects over an eight-year period, from 2008 to 2015. It will now strive to review the ongoing projects, making sure that they achieve all their targets, as they run to completion.

2.2. Events

2.2.1 European Nanoelectronics Forum 2015 and CATRENE Innovation Award

The European Nanoelectronics Forum 2015, which took place in Berlin, Germany on 1-2 December, was jointly organised by AENEAS, CATRENE, the ECSEL Joint Undertaking and the European Commission.

More than 280 participants from all over Europe attended the event that had as its theme, “Driving Digital Economy”. Hosting the plenary sessions were highly-qualified keynote speakers from within the micro- and nanoelectronics-based eco-system, who were once again appreciated.

The Project Village, which occupied a 1400 m² area, comprised 62 projects representing CATRENE, the ENIAC JU and the European Commission’s FP7 programme. Its setup and space were ideal for discussions and networking. The three “Speakers Sessions”, held right next to the exhibition area, created an informal setting to present and discuss hot topics. The number of participants at these sessions – some 80 people – remained at the same level as 2014.

Feedback in the questionnaires sent to participants at the end of the Forum reflected a high level of satisfaction (with 80% of expectations met). However, participants did suggest that keynote speakers should be more diverse next year.

One of the Forum’s highlights was the CATRENE Innovation Award, which went this year to the NewP@ss project. This annual award is bestowed on a project with a high level of innovation and far-reaching exploitation potential, market impact and overall benefits for Europe, as well as, creative objectives and effective management.

And there were good reasons why its win was justified. NewP@ss reflects the needs of the next generations of e-Passport currently under discussion at the International Civil Aviation Organisation (ICAO), and their use to facilitate travel and provide access to e-Services. Its advanced, secure passport platform embeds state-of-the-art, near-field communication capabilities and is 16 times faster than the generation of passport currently in use. In addition, the NewP@ss platform has reached the highest level of security required for border-control operations. (A full description of NewP@ass can be found in Section 3.2.6 of this report.)

The next European Nanoelectronics Forum will be held on 23-24 November 2016 in Rome.

2.2.2 CATRENE Scientific Committee Workshop on Smart Cities

See 2.3.2

2.2.3 CATRENE Design Technology Conference 2015

The CATRENE Design Technology Conference (DTC) was held on May 19th and 20th 2015 in Dresden, Germany. It was co-located with the edaWorkshop15, with which it shared keynotes, sessions and a social event. Both events are attracting European experts in industry and academia, which has led event organisers to co-locate the workshop and the conference every two years. The conference, which had nearly 100 participants, creates ideal opportunities for a professional exchange of ideas grounded in the latest scientific advances in the field.

The 2015 CATRENE DTC was organised into six technical sessions:

1. Connected Objects
2. Energy Efficient MP SoC
3. Modelling and Simulation
4. FDSOI Ecosystem
5. Security, Safety and Privacy
6. V2X : Car to Environment Communication

It is important to place such a conference in perspective. Held annually, the CATRENE DTC has become the meeting point for Europe's scientists and experts in applications-oriented design. It is a unique opportunity to meet the CATRENE project researchers, while taking advantage of the conference's high quality programme. Notably, attendees all agree that the best thing about the DTC is the technical results presented by real experts from the field. And the confluence of academic and industrial perspectives, as well as, those from electronic system design and manufacturing, makes the CATRENE DTC unlike any other similar type of conference.

2.3. Publications

2.3.1 Project profiles and result sheets








2.3.2 Catrene Scientific Committee Report on Smart Cities

During 2014, the CATRENE Scientific Committee conducted a study on “Semiconductor Technologies for Smart Cities” with the goal to identify the need for micro- and nanoelectronics and smart systems for use in “Smart Cities”. The report was designed as the first phase in the investigation of Smart Cities, to be complemented with concrete use cases at a later date. It was released in January 2015 and presented at a workshop on April 14 that year in Brussels. About 50 participants attended the presentations and discussed which micro- and nanoelectronics-based components and systems will be essential for Smart Cities.

Smart Cities can be interpreted as a “system of systems”, connecting a huge number of microelectronic applications, and using a large number of sensors, sensor networks and communication infrastructure. This means Smart Cities will be a use case of the so-called internet of things (IoT). Sensors will become the “eyes and ears” of a smart city; and sensor networks will be the “nerves” which feed the “brain” (ICT infrastructure) with the necessary data to monitor and simulate all relevant urban processes. The outcome of the simulations will be used to control production, traffic and logistics within the urban environment.

Within the concept of Smart Cities, three major domains have been identified with having a strong need for semiconductors which will be relevant to the European semiconductor industries:

1. Smart, energy efficient (autarkic) sensor systems
   (cyber-physical systems) at low cost (edge computing / instant data);
2. Highly efficient and secure communication infrastructures
   (networks & processing capabilities for the Cloud / Big Data);
3. Sufficient power supply to run this new infrastructure
   (energy supply and ultra-low / zero-power systems).

2.4 Press Coverage

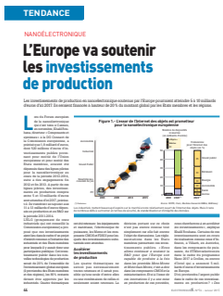
July 2015

"NewP@ss" Research Project Boosts Security Technologies for Next Generation ePassports and eGovernment Applications

http://www.nxp.com/news/press-releases/2015/07/newpass-research-project-boosts-security-technologies-for-next-generation-epassports-and-egovernment-applications.html

January 2015

L'Europe va soutenir les investissements de production


TENDANCE

NANOÉLECTRONIQUE

L'Europe va soutenir les investissements de production

3 Review of Call 8 and projects ended in 2015

Call 8 at a glance

A total of nine project-outlines, leading to four full proposals, were received in the 2015 CATRENE Call 8. Out of these four projects, three were labelled as CATRENE and one as ECSEL.

CATRENE Call 8 projects amounted to a total effort of 571 PYs. The highest country-contribution is Germany's with 32% of the combined effort, followed by contributions from France with 30% and the Netherlands with 15% (see Figure 1).

Figure 1: Share by country of the total effort (in PYs) of operational Call 8 projects

In Call 8, only application-related projects were labelled, with a focus on Automotive. In particular, the upgrade of consumer electronics technologies for Advanced Driver Assistance Systems and Connected-Cars applications, has been greatly supported by the CATRENE public authorities. Healthcare (with the development of new body monitoring sensors), and Design (with the development of a parallelisable and interoperable simulation framework), were the two other work-areas labelled during this call.

From a technology perspective, it is noted that the project REFERENCE, which focused on highly innovative silicon-on-insulator (SOI) substrates for radio frequency (RF) applications, was initiated in CATRENE. Its flexible and iterative process, together with strong support of the reviewers and mentor, led to a high-quality project proposal, which has been implemented in the ECSEL environment.

Completed projects

During 2015, six projects were completed, a majority of which belonged to the 4th Call of CATRENE.

More details on projects in part 3.2.

Call		Index	PYs	Patents	Dissemination
3 CT209	Semiconducor process and integration [RF2THZ-SiSOC]	3.2.2	235	6	240 contributions to international conferences and publications, 3 PhD thesis
	Contribution to standardization Industry standard HiCUM/L2 HBT compact model : RF2THz hardware from ST and feedback from circuit design have allowed TUDD to validate the model for advanced SiGe HBT technology and to identify relevant improvements				
4 CA109	Communication & Digital Lifestyles [SHARP]	3.2.3	64	3	18 technical papers, 3 PhD thesis
	Contribution to standardization Contributions to standards PCIe (SW/HW co-validation), MPA and PGAS (HPC/server software), SystemC (system-level verification), and Linux (many-core OS)				
4 CA701	Design technology [H-INCEPTION]	3.2.4	92	0	8 participations at events, 29 publications and 9 trainings
	Contribution to standardization Participation in 4 working groups in the Accellera and IEEE committees, with key contributions in SystemC MDVP (Multi-Domain Virtual Prototyping) and IP-XACT MDVP				
4 CA110	Communication & Digital Lifestyles [APPSGATE]	3.2.5	178	0	Over 10 papers
	Contribution to standardization As participant of the W3C Model-Based User Interface Working Group, UJF/LIG has contributed to the standardization of languages for describing user Interfaces at multiple levels of abstraction from task modeling to concrete user interfaces.				
4 CA206	Safety and security [Newp@ss]	3.2.6	170	2	13 presented conference papers, 1 journal article
	Contribution to standardization The project allowed contributions to the following international standardization bodies : ISO JTC1 SC17, SC27, and ISO/IEC 7816; ICAO NTWG and ICBWG; GlobalPlatform Government Task Force, Card, and Device committees; European Commission DG Home art6; CEN/TC 224; ETSI SCP; NFC Forum; Java Card Forum; ISCI and JHAS				
4 CA310	Automotive and Transportation [EM4EM]	3.2.7	91	6	18 technical papers, 3 PhD thesis
	Contribution to standardization “The transfer of EM4EM results to standardization bodies is in progress. An example will be the decoupling measurement method for electrical machines in GAKAK767.13/. 14/.18.”				

3.1 Call 8 projects (labelled in 2015)

3.1.1 Overview table

Call			Index	PYs
8	CAT311	Automotive and Transportation [TRACE]	3.1.2	260
8	CAT408	Health and the ageing society [NexGen]	3.1.3	160
8	CAT602	Design technology [PARADISE]	3.1.4	151

3.1.2 PROJECT

CAT311

Enabling smart mobility and smart infrastructure by developing a technology readiness process for consumer electronics. [TRACE]

COUNTRIES INVOLVED & PARTNERS

Austria

ams AG / FH JOANNEUM GmbH /NXP Semiconductors, Aut Semiconductors Austria GmbH

France

AKKA Informatique et Systèmes / CEA – Leti / Continental Automotive France SAS / Coventor / IMS lab / OpenWide / SILKAN RT / ST Microelectronics / STATXPERT / STMicroelectronics SA / STMicroelectronics Fr / Tronics Microsystems / vehicle program

Germany

Berliner Nanotest und Design GmbH / BMW AG / Chemnitzer Werkstoffmechanik GmbH / Daimler AG / Fraunhofer – ENAS / FRT GmbH / GOEPEL electronic / iMAR Navigation GmbH / NXP Semiconductors, De / Robert Bosch GmbH / Siemens / TWT GmbH Science & Innovation / UHB - University of Bremen / University of Siegen / Volkswagen AG AG

The Netherlands

Catena Holding / Heliox / NXP Semiconductors, Nl / TUD - Technical University Delft

Sweden

Imsys AB / KTH Royal Institute of Technology / QRTECH AB / Swerea IVF AB Volvo Car Corporation

PROJECT LEADER

Jochen Beintner
Robert Bosch GmbH, Germany

EXPECTED START DATE

01 April 2016

EXPECTED END DATE

31 March 2019

Brief description of the project goals

Smart mobility – of which self-parking, self-driving, and connected vehicles are good examples – requires extremely powerful processing power, high-precision sensors and seamless integration of high-performance mobile wireless devices. These innovative automotive applications depend on complex semiconductor devices. As fab, technology-development and chip-design costs increase with the introduction of more advanced technology nodes, amortisation needs increasing volumes which are not covered by the automotive electronic market alone.

Hence, in future technology nodes, only those semiconductor manufacturers who can fully use the economy of scale of the communication, computer, and consumer markets, will be able to handle the tremendous investments required for these nodes. Consequently, innovative and affordable automotive systems that require complex semiconductor devices will only become a reality in the near future if the functionality available in consumer semiconductor devices can also be made available to the automotive domain.

However, the deployment of consumer semiconductor components will encounter (and need to overcome) a massive obstacle: in most cases, the consumer semiconductor components do not meet automotive requirements for quality, reliability, safety, robustness, as well as, service levels and long-term supply.

Project TRACE aims at developing a method (including processes and tools) to upgrade consumer electronics (CE) components and technologies, and qualify their transfer to the automotive domain. The structure of this method will be based on an iterative requirement: an engineering process integrating risk-management analysis. Incremental measures or changes required for qualification are analysed transparently and jointly within the whole automotive value-chain. This is done by holistically considering the consequences at a component, system-integration and application level.

In particular, the project will deal with:

- Requirement engineering process: The purpose is to allow the transition from the actual top-down approach to a value-chain one;
- System Integration: To “robustify” the CE component, the following solutions will be investigated: redundancy, diversity, data fusion, self-calibration, diagnosis, advanced statistical methods and replacement;
- Component upgrade: Component modification will include: enhancing semiconductor process technologies; circuit design (design for X, which means the design methodology can be used for different applications) and layouts; package technologies; and adapting tests on a wafer or module level to prove effectiveness of modifications;
- Test and validation: Increase the test coverage of CE and develop new test techniques;
- Simulation: physical CE electronics models that work within automotive;
- Economics: Replacement problems, cost models and standardisation;
- Demonstrators: Addressing a representative base of automotive applications, relying on the usage of upgraded CE semiconductor component (safety-critical and non-safety critical). These will include detection and ranging, navigation and autonomous infrastructure interaction.

3.1.3 PROJECT

CAT408

Next generation of body monitoring. [NexGen]

COUNTRIES INVOLVED & PARTNERS

Belgium

NXP / Quad Industries / SIOEN Industries

Finland

Enfucell Oy

Germany

B. Braun Melsungen AG / Charité - Universitaetsmedizin Berlin / eesy-id GmbH / IFD / IHP - Innovation for High Performance Microelectonics / Infineon Technologies AG / InnoRoute GmbH / senetics healthcare group GmbH & Co. KG / Siemens / Wearable Technologies AG

The Netherlands

Evalan / Imec Stichting IMEC Nederland / Maastricht Instruments / NXP Semiconductors / PHILIPS Electronics Nederland B.V. Research Research

PROJECT LEADER

Tanja Seiderer
Infineon Technologies AG, Germany

EXPECTED START DATE

01 April 2016

EXPECTED END DATE

31 March 2019

Brief description of the project goals

Mobile health-care systems, based on a multitude of different networked sensors that enable ubiquitous body monitoring, are seen by world-leading industry and health-care suppliers as a key solution to address chronic diseases – especially multi morbidity (co-occurring diseases) – by improving the quality of medical services and making elderly people more independent. New mass markets will emerge and nanoelectronic-based components will be available to secure these mobile medical electronic solutions at reasonable costs. However, there are challenges that limit the benefits of eHealth today and hinder a swift and successful commercial launch. These are the challenges of economic risk, market fragmentation and limitations of current micro- and nanoelectronic technologies and several missing components (such as sensors and energy harvesters; standardised protocols; security blocks; and integration technologies for biocompatible and implantable solutions).

The Nextgen project (the name stands for Next Generation of Body Monitoring) aims to develop key microelectronic technologies and components for future mobile/wearable health-care systems. Their feasibility will be demonstrated using two interconnected, ubiquitous body-monitoring systems of high social and economic importance: an implanted glucose monitor and a non-invasive, on-body, multi-parameter monitor. It will confirm that these body-monitoring systems facilitate new business cases in mobile health care.

Target technology achievements are:

- Sensors for body monitoring of: motion; dehydration (RF sensor measuring up to 30GHz); glucose (ultra-wideband RF sensor up to 100GHz); chemicals (for example, pH, Cl-, Na, K+); and impedance and temperature;
- Components to improve system energy management: wake-up features; low-power circuits, motion- energy harvesters; integrated silicon- based micro batteries; and integrated printed disposable batteries;
- Communication and security components: NFC/RFID and related antennas; RF communication; and on-chip security blocks.;
- Biocompatible integration technologies for medical applications: 3D integration with TSVs and interposer (system size: 0.01cm3); and flexible substrate (less than 500µm system thickness) non-metallic hermetic encapsulation;
- Multivariate signal evaluation: by using linear as well as nonlinear algorithms for eliminating cross influences.

3.1.4 PROJECT

CAT602

Parallel and distributed simulation environment. [PARADISE]

COUNTRIES INVOLVED & PARTNERS

Austria

CISC Semiconductor GmbH

Finland

Microteam Oy / Nokia Networks / Siru Innovations Oy / Tampere University of Technology

France

Bull SAS / CEA / Magillem Design Services / METASymbiose SAS / STMicroelectronics / Université Joseph Fourier/CNRS LIG / UPMC / LIP-6 / Verimag

Spain

IKERLAN Ikerlan S. Coop / Thales Alenia Space / University of Cantabria

PROJECT LEADER

Laurent Maillet-Contoz
STMicroelectronics

EXPECTED START DATE

04 April 2015

EXPECTED END DATE

27 September 2019

Brief description of the project goals

The PARADISE project aims to provide a scalable solution that systematically fulfils the two main needs in complex system simulation: easy model integration; and high execution speed. Facilitating integration is crucial to save design time, as today's system components and their respective simulation models are inherently heterogeneous. Surmounting the simulation-speed challenge (caused by the continuous increase in complexity, heterogeneity and size of designed systems) should result in a scalable and long-term solution for the dynamic verification of these complex systems.

In order to reduce simulation time, manage the design complexity of heterogeneous systems, and facilitate virtual prototypes integration, Paradise will develop new methods and tools based on distributed and parallel simulation techniques.

The first goal of this project is the definition and development of a modular and parallel/distributed simulation framework. Its specific design will ensure its scalability, thanks to the existing massively parallel-processing environments. Four computing platforms are being considered: SHARP (heterogeneous HPC platform), LSF farm, FPGA board and Cloud computing.

The second goal is the definition and implementation of a simulation backbone to support the communication and synchronisation of diverse simulators hosted on distributed computing nodes. It will provide the appropriate functions and interfaces to support straightforward interconnection of different types of simulators, simulating at different levels of abstraction. Modelling guidelines will be issued to support the development of a model portfolio compatible with the PARADISE parallel and distributed simulation framework.

The third goal is to develop a variety of tools to facilitate the development, debugging and validation of parallelisable models, as well as, the evaluation of distributed simulation performance. The fourth and final goal is to validate these implementations and evaluate the results of the project on different case studies provided by the industrial project partners. Targeting open solutions, effort will be made to contribute to the standardisation of the services of the parallel and distributed simulation backbone.

The main outcomes of the project are a distributed simulation backbone, providing unified access to computing resources; a set of interfaces to access the services provided by the backbone; guidelines to develop easy-to-integrate models; a model portfolio to initiate an industry-wide ecosystem; and tools to support parallel programming, debugging and profiling activities on parallel simulations.

The project consortium covers a wide part of the value chain, ranging from semiconductor companies and system houses, to tool vendors and academia. The technologies developed in the project will directly benefit the project partners throughout the value chain, and indirectly their customers. Creating efficient simulation of complex heterogeneous systems is a major expectation shared by all stakeholders, and a key factor for validating extremely complex systems in order to reduce development time and cost, and guaranty high-quality designs.

3.2 Projects ended in 2015

3.2.1 Overview table

Call			Index	PYs
3	CT209	Semiconducor process and integration [RF2THZ-SiSOC]	3.2.2	235
4	CA109	Communication & Digital Lifestyles [SHARP]	3.2.3	64
4	CA701	Design technology [H-INCEPTION]	3.2.4	92
4	CA110	Communication & Digital Lifestyles [APPSGATE]	3.2.5	178
4	CA206	Safety and security [Newp@ss]	3.2.6	170
4	CA310	Automotive and Transportation [EM4EM]	3.2.7	91

3.2.2 PROJECT

CT209

System-on-chip technologies for emerging consumer applications: Radio Frequency, Millimeter-Wave and Terahertz [RF2THZ-SiSOC]

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Newtec Cy N.V.

Germany

Alcatel-Lucent / Robert Bosch GmbH / IHP - Innovation for High Performance Microelectonics / Agilent Technologies / Fraunhofer / University of Siegen / Technical University Berlin / TU-Dresden / Micram Microelectronic GmbH / Saarland University / Silicon Radar / Synview

France

STMicroelectronics / NXP / ESIEE / IEMN / ENSICAEN / ASTUS / IMS / CEA / IES - Institut d'Electronique du Sud / XMOD Technologies / Telecom Bretagne / Institut Polytechnique Grenoble (INP)

The Netherlands

TUE - Technical University Eindhoven / Axiom IC / NXP / Salland Engineering / MASER Engineering B.V. / Bruco Integrated Circuits / TUD - Technical University Delft

PROJECT LEADER

Jean-Louis Carbonero

START DATE

01 July 2011

END DATE

31 December 2015

Brief description of the project goals

The RF2THZ-SiSoC project has led to the establishment of silicon technology platforms for emerging Radio Frequency (RF), Millimeter-Wave (MMW) and Terahertz (THz) consumer applications, such as:

- 77GHz/120GHz automotive radars;
- MMW imaging and sensing;
- Fast measurement equipment;
- 60GHz wireless networking and fast downloading Rx/Tx, 400Gbit/s optical data communications;
- 4G photonic mobile communication transceiver and RF wireless communication requiring high- performance devices (transmitted power, consumption, integration, isolation);
- Two-way satellite communication systems.

The large project consortium (33 partners from four countries) covered the full supply-chain disciplines/activities: semiconductor processes, characterisation, modelling, reliability, design, test, and applications with academics and industrial partners. The good cooperation between all partners was key to the project's success. The RF2THz project has generated more than 140 internal documents, kits, tape-outs, silicon-outs, models and devices exchanged between project partners. The quality of the highly scientific work has been recognised internationally, thanks to six patents, activities in standardisation, and 240 contributions to international conferences and international publications.

The first products based on the RF2THZ-SiSoC platforms are available on the market. As early as end-2014, more than 20 customer tape-outs using the BiCMOS55 technology platform were released. This technology is now available at the right maturity level for production. In parallel, Élite passive devices were successfully integrated into NXP's newest BiCMOS platform addressing , active antenna applications (cellular, base stations, satcom). All but two demos (not completed due to challenging issues) were ready by the end of the project and were able to demonstrate its outstanding results.

3.2.3 PROJECT

CA109

Scalable heterogeneous architecture for processing [SHARP]

COUNTRIES INVOLVED & PARTNERS

Germany

FZI - Forschungszentrum Informatik

France

Bull SAS / UPMC / LIP-6 / Thales / CEA

PROJECT LEADER

Huy Nam Nguyen
BULL

START DATE

01 September 2012

END DATE

30 August 2015

Brief description of the project goals

Project SHARP's overall goal was to develop a heterogeneous high-performance computer (HPC) architecture that reflected a market evolution. Looking back at the development of the HPC – from teraflops (1997) up to petaflops (2008), and with the deployment of exascale systems by the TOP500 supercomputer users on the horizon in 2018 – the number of processing cores is expected to increase dramatically, soon to reach a range of between 10^5 and 10^6 elements. Since 2008, the race to achieve ever-higher performance has led HPC developers to experiment heavily with accelerators, GPU, FPGA and embedded technology. In fact, current HPC hybrid architecture integrates general-purpose (many/multi-core) CPU- and GPU-type cores with FPGA, resulting in the next add-on to support a larger range of applications requiring a variety of fine-grain parallelisms (referring to the Berkeley classification).

SHARP contributed significantly to this evolution with the investigation and prototyping of HPC hybrid architecture as an extension of the existing BullX HPC system, together with the design of the many-core TSAR processor using a 2.5D-silicon technology. At the application level, the growing number of heterogeneous computing components within the hardware architecture also required a larger effort to parallelise algorithms, and porting existing sequential codes to the hybrid HPC architecture was another SHARP contribution.

SHARP's major technical achievements include:

- Designing and prototyping a generic HPC architecture that integrates a variety of computing technologies (many-core CPU, GPGPU, FPGA);
- A complete design of the TSAR processor in a 2.5D silicon technology (tape-out);
- Software development (OS, specific application layers, etc.) in relation to various computing technologies and to support security features;
- An optimal implementation of a large range of applications of heterogeneous computing technologies: Examples include video processing (multi-core CPU+FPGA); traffic-light recognition (many-core CPUs); medical image processing (CPU+GPU); and system prototyping (CPU+FPGA).

Many of these developments go far beyond their initial objectives: they can be applied to real-life industrial issues (such as HPC components; industrial exploitation of prototypes, tools and methodologies; and educational materials). This demonstrates both, the passion with which the work was done and the efficiency of the results. All work packages kept to the FP schedule throughout the project, and their respective deliverables are now available.

In terms of dissemination, SHARP generated three patents, four PhD theses (with two more still being worked on), and published 18 technical papers.

There was very close bilateral and multilateral cooperation between project partners, and collaboration with external partners/projects that was both necessary and very fruitful for a relatively small-sized project.

Finally, developments from SHARP have been deployed in many subsequent European or national projects.

3.2.4 PROJECT

CA701 | Heterogeneous Inception [H-Inception]

COUNTRIES INVOLVED & PARTNERS

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Ecole Polytechnique Federale de Lausanne

France

STMicroelectronics / UPMC / LIP-6 / Continental Automotive / Coventor / Magillem Design Services / Atrenta / Ecole Centrale de Lyon

The Netherlands

Dizain-Sync / Imec / TUD - Technical University Delft / Reden / Oce Technologies / Smart Signs Solutions

Spain

Brio Apps AlphaSIP

PROJECT LEADER

Olivier Guillaume
STMicroelectronics, France

START DATE

10 December 2012

END DATE

31 December 2015

Brief description of the project goals

The H-Inception project delivered a unified design methodology and tools to address virtual prototyping of heterogeneous systems.

This helps industry perform system-level design and verification very early in the product development flow, and helps decrease time to market and cost for such systems.

Indeed, recent technological advances have led to a broad range of emerging applications of microelectronic systems with embedded software that interacts with the surrounding environment involving various physical domains (such as optical, mechanical and biological). Conventionally, architectural studies are done separately in the different domains. This leads to design errors discovered late in the design cycle and thus requiring design re-spins (re-design with improved parameters).

H-Inception made use of a framework with a simulator that validated seven use cases covering five domains of activity: Wireless, Consumer Electronics, Automotive, Medical and Printing. For instance, it demonstrates how optimising the injector system can reduce vehicle CO2 emissions. Another example is the cost and development-time reductions by a factor of two of a biomarker lab, thus facilitating its deployment for cardiac-disease detection.

Key to the success of the project was the re-use and the extension of two standardised computer languages widely used in the industry for digital systems with embedded software. These languages are SystemC for simulation, and IP-XACT for model management and flow automation. BeyondDreams, a CATRENE project, which ran between 2009 and 2012, extended their capabilities to analogue and mixed systems. In H-Inception, the work on the SystemC extensions allowed the use of a simulator with new models of computation, such as Bond Graph for mechanics and SPH for fluidics. The work on the IP-XACT extensions made possible a framework for integrating all steps, from schematic entry to simulation, including checking. This framework can now be used by all system engineers, regardless of their competencies. The standardisation efforts, started in BeyondDreams, were pursued in H-Inception through the participation in four working groups in the Accellera and IEEE committees.

The use of standards increases the competitiveness of our solution. Indeed, a single-kernel simulator, based on SystemC extensions, avoided the need for multiple simulators and their related licence cost. Furthermore, thanks to IP-XACT, the database is not proprietary and can be easily shared.

Information-sharing within the H-Inception consortium was excellent. There were 56 on-time deliverables, five face-to-face meetings and 34 monthly teleconferences. Furthermore, the project consortium collaborated on three other projects (OpenES; Verdi and SMAC) with joint papers, and participation in deliverables and methodology improvement.

Project members were also active disseminating project results: eight participations at events; 29 publications; and nine training sessions. Another outcome that will facilitate the dissemination of SystemC-AMS extensions for the multi-domain is a library of model examples (including 37 models, associated documentation and test benches).

The simulator is now available and can be downloaded freely from the H-Inception website. Industrial partners are already deploying the methodology in the development of new products. Encouragingly, an evaluation showed a cost reduction of up to 60% for prototyping, and a reduction in design time of six months. EDA partners are integrating the project outcomes in their tool offerings and services. And partners from academia already promote the computer languages in their courses. Finally, the results will be reused in new collaborative projects: Paradise (simulation parallelisation), SylverPlaces (verification and UVM) and VIRTUO (MEMS, IoT).

3.2.5 PROJECT

CA110 | Applications Gateway [AppsGate]

COUNTRIES INVOLVED & PARTNERS

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SoftKinetic Sensors / SoftKinetic Software

France

STMicroelectronics / NXP / PACE France / Technicolor / LIG LAB / 4MOD Technology / ARD - Alpes Recherche et Developpement / Ripple Motion / Immotronic / Institut Mines-Telecom / Telecom ParisTech

Spain

Video Stream Networks, S.L. / Simon Tech

PROJECT LEADER

Jean-Christophe Pont

START DATE

01 September 2012

END DATE

30 June 2015

Brief description of the project goals

The AppsGate project was born from the idea that the latest set top boxes (STBs) with their huge computing power could do much more than only provide multimedia services. In fact, a new world of integrated home services could be created if STBs were equipped with open-software frameworks and a large selection of high bandwidth/low power connectivity standards.

This led to the formation of the AppsGate project consortium, comprising chip suppliers, consumer electronics OEMs and service providers, with the purpose of demonstrating advanced STBs supporting home automation, energy management and health-care applications, seamlessly integrated with legacy STB services.

The consortium quickly realised that no single software-framework available would address every need and requirement. A software stack had to therefore be devised to best fulfil broadcast, broadband and smart home requirements, even at the expense of some integration complexity.

Broadcast is addressed by STB middleware from Pace and Technicolor. This software was designed to provide the best quality TV services by using multimedia hardware features embedded into the STB chips. Broadband is handled by the Android operating system, which provides instant access to countless apps and over-the-top services (delivered over the Internet and without the involvement of a multiple- system operator), and which offers a framework for monetising new ones.

Smart home posed a unique set of challenges. The system had to be able to identify new services and adapt to devices coming online and going offline. In addition, the system needed to manage diverse communication protocols and exchange information and services. In the absence of any widely adopted standard, AppsGate took two complementary approaches, based on technologies available from the consortium partners. The first approach is architected around a message bus based on Technicolor's Qeo technology. The second one implements a service broker using ApAM (Application Abstract Machine),a technology developed by UJF/LIG on top of OSGi.

End-to-end security and data privacy were major concerns that were tackled using technology developed to protect premium content in STBs. Usability, another concern, was considered early on in the project since it drives system acceptance. Natural language is, for instance, used by end-users for specifying home automation scenarios. The main challenge of AppsGate was the integration of a deep technology stack with a large number of interfaces. To address this issue, clusters of partners were formed around each hardware platform. This concept of a "cooperation cluster" proved very effective by simplifying interaction. It also enabled a tighter integration of partner technologies than was initially envisioned, and generated new ideas that were readily implemented.

AppsGate has its share of successes. The first products based on AppsGate technologies are reaching the market. The most notable is Cube S from Canal+, developed by Technicolor around ST's system-on-chip. More Android STBs from Technicolor and Pace are expected to follow. ST has also secured customers for the cable gateway, bundled with NXP's Full-spectrum Transceiver. 4MOD is shipping the BLE remote control, and the 6LoWPAN is under evaluation with huge-volume prospects. Simon Tech will unveil a new line-up of Z-Wave products for its centennial. ARD, Immotronic, SoftKinetic and VSN will use the expertise developed in the project to strengthen their product roadmap. IMT and UJF/LIG have published more than 10 papers, and the AppsGate Smart Home, installed in INRIA's Rhône-Alpes living lab, will be used for further research.

3.2.6 PROJECT

CA206 | [NewP@ss]

COUNTRIES INVOLVED & PARTNERS

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Graz University of Technology / NXP / Semiconductors, Aut / Infineon Technologies, Aut

Germany

Giesecke & Devrient / Infineon Technologies AG / NXP

France

STMicroelectronics / Gemalto SA / NXP / id3 Technologies / CEA / ISEN – Toulon

Hungary

Compuworx Corporation

Portugal

Evoleo Technologies / Instituto de Telecomunicacoes

PROJECT LEADER

Michael GUERASSIMO
Gemalto

START DATE

01 July 2012

END DATE

30 June 2015

Brief description of the project goals

The NewP@ss project delivered advanced secure platforms (microelectronics and embedded software) suitable for the upcoming third and fourth generation of e-Passport, which are currently under review at the International Civil Aviation Organization (ICAO).

The e-Passport could be used as an approved travel document at a European and International level, and also be deployed for hosting dedicated e-services applications for both government (an electronic visa, for example) and/or private organisations (consider boarding-pass support, airline services and the like).

These advanced secure passport platforms embed state-of-the-art, near field communication (NFC) capabilities, making them 16 times faster than the generation of passport currently in the field. The world's fastest electronic passport and corresponding reading equipment were demonstrated as part of this project. This passport will help automate and speed up border crossing (and facilitate the weary traveller) though the use of the fast VHBR contactless communication protocol.

Secure microcontrollers were developed to provide the necessary advanced computing power and memory for the highest performance in high-security applications. Associated readers were also developed to ensure good performance and interoperability. With the increase in fraud, special focus was placed on security and privacy aspects through the development of new cryptography protocols (such as SAC or EACv2.1). In fact, the NewP@ss platform has the highest level of security required in border control.

Information sharing within the NewP@ss consortium was excellent. More than 50 reports (containing project results) were shared internally, and new collaborations established. NewP@ss partners also shared newly acquired knowledge and scientific results in academic journals and at major international conferences. In addition, the consortium contributed to various meetings related to eMRTD document and security standards, such as LDSv2 standardisation that provide new data groups for storing eVisas, eTravel Stamps and eBoarding Pass. Intensive cooperation between all the partners continued during the project. Over 14 demonstrators and four complex use cases demonstrators were defined (working in a collaborative mode) to illustrate border control and eTraveler journey use cases.

The 3G e-Passport developed in the project is now available and will be delivered to customers starting in 2016; and the 4G e-Passport from 2018. VHBR technology will be improved in the coming years and implemented in smartphone and tablets. All the cryptographic protocols will be reused and improved for deployment in other electronic documents, such as eID or ePermit resident. These new features will not only make travelling abroad easier for e-Passport holders, but also give them access to public or private digital e-Services.

These new e-Passport technologies represent a complete paradigm shift, demonstrated in the project through innovative technology concepts (such as a high-speed interface, a multi-application embedded software platform, on-card components display and the like), mobile applications and readers.

Fifteen project partners from five countries involved in EUREKA worked on the project concept and realisation, and, in particular, addressed interoperability at application level; developed test tools; and provided proactive input to standards organisations.

NewP@ss contributed to the Grand Challenge “Consumer and Citizens Security”, which is part of the AENEAS/CATRENE vision, mission and strategy. This project was made possible through the support of the CATRENE programmes. The applications targeted by Newp@ss have important economic, societal and technical impact, and should represent a significant part of the e-Passport market by 2015-2020. Importantly, these applications share some of the compelling security and interoperability needs at a European and international level.

3.2.7 PROJECT

CA310

Electromagnetic reliability of electronic systems for electro mobility [EM4EM]

COUNTRIES INVOLVED & PARTNERS

Germany

University of Hannover / Audi / Infineon Technologies AG / Robert Bosch GmbH / Zuken GmbH / TU Dortmund / NXP / FAU - University of Erlangen-Nurnberg / Daimler / Elmos Semiconductor / Conti Temic microelectronic GmbH

Finland

VTT Technical Research Centre of Finland Ltd / Okmetic / MURATA

Czech Republic

IMA s.r.o. / Brno University of Technology

PROJECT LEADER

Joern Leopold
Audi

START DATE

01 July 2012

END DATE

31 March 2015

Brief description of the project goals

Future electrically operated vehicles will encounter many huge design challenges with electric and electronic devices at all levels: application, vehicle, system, component and semiconductor. The close vicinity of high-intensity fields generated by high-power cables and electric motors, and sensitive high-density electronics, require a holistic approach to both, electromagnetic compatibility (EMC) and electromagnetic reliability (EMR).

In order to address these EMC/EMR issues, the EM4EM project developed methodologies, measurement methods and stable transmission line-modelling methods (including simulation tools). In addition, a set of 26 demonstrators for the four application tiers were built for validation purposes, and for use in developing the first products based on the technology developed in this project.

Some of EM4EM's many major technical achievements include:

- The development, at the semiconductor level, of a new IGBT (insulated-gate bipolar transistor) module design with a reduction in noise level;
- The development of a new BCI (bulk current injection) setup for measuring an extended frequency range between 100 kHz and 400 MHz;
- The development and testing, at the component level, of a new ringing active control method for PWM (pulse width modulation) driver transistors (based on a ringing measurement without the time- consuming calculation based on a fully adaptive algorithm);
- The development and integration, at the system and vehicle levels, of innovative new algorithms to suppress EMI (electromagnetic interference) in an integrated tuner for AM, FM and DAB broadcast services. The latest measurements show that the SNR was improved by about 10 to 25 dB. The integration and demonstration is currently being done by a European chip supplier;
- The introduction of a new measurement methodology to define the initial EMR condition for HEV/PHEV/EV (automotive requirements regarding electromagnetic compatibility of electronic components). For example, conducted current measurements of a high-voltage system on HV, LV and ground interfaces;
- Research, on the material level, on another essential part of the project: to qualify suitable lightweight materials (CFRP: carbon fibre reinforced polymers) in order to reduce weight and ensure the electromagnetic shielding is effective. The resulting weight reduction by using compact and efficient devices is essential in addressing environmental challenges in terms of CO2 emission.

Key to the success of the EM4EM project was its use of the four tiers of the value chain – semiconductor, component, system and vehicle – in order to leverage economies of scale. Thanks to the newly introduced research teams across the work package, internal R&D cooperation and information sharing within the EM4EM consortium was excellent and very efficient. This broad range of cooperation between industrial partners (as a part of the four tier approach) and those from academia was only made possible by the support of CATRENE and the national funding bodies involved.

There was good information sharing and dissemination in the project. A number of reports (more than 1600 pages) containing all project R&D results were internally exchanged, and new collaborations established. Knowledge gained from the project was also shared with academia and industry. More than 57 papers were written; four workshops organised; 78 presentations given; 28 posters presented; and six patent applications submitted. In addition, four awards were received: the EEEfCOM Innovation Award 2012 (2nd Place); ESD Forum 2013; EMC Tokyo 2014; and the CATRENE Innovation 2014 Award.

4 Appendices

APPENDIX A

CATRENE People Finder

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APPENDIX B

CATRENE Projects Focus Matrix

The CATRENE Projects Focus Matrix identifies the work areas addressed by each project. A maximum of 5 *s can be allocated to a single project. A * indicates that the project addresses the work area in question, with this focus growing with each additional *.

PROJECT	Communication & Digital Lifestyle	Safety & Security	Automotive & Transport	Health and the Ageing Society	Energy Efficiency	Design Technologies	Semiconductor Process & Integration	Equipment, Materials & Manufacturing
CAT602 [PANAMA]	**				*			
CA103 [HERTZ]	**				*			
CA104 [COBRA]	***					*		
CA109 [SHARP]	*			*		***		
CA110 [APPSGATE]	**			*	*			
CA111 [UltraHD-4U]	***							
CA112 [HARP]	**		*		*	*		
CA114 [WiCon]	***						**	
CA116 [CORTIF]	***							
CA118 [FITNESS]	***					**		
CA202 [eGo]	*	***						
CA206 [NewP@ss]		***						

PROJECT	Communication & Digital Lifestyle	Safety & Security	Automotive & Transport	Health and the Ageing Society	Energy Efficiency	Design Technologies	Semiconductor Process & Integration	Equipment, Materials & Manufacturing
CA208 [MobiTrust]		***						
CA301 [HiDRaLoN]	*		*	*				
CA303 [OPTIMISE]			**		*	**		
CA308 [ICAF]	***	**						
CA310 [EM4EM]			***			**		
CA402 [THOR]			*	*	*	*		
CA403 [RELY]			*	*		***		
CA501 [COMCAS]	**				**	*		
CA502 [SEEL]			**		***			
CA505 [BENEFIC]	*				**	**		
CA507 [GREETINGS16]					***	**		
CA701 [H-INCEPTION]						***		
CA703 [OpenES]	*		*			***		
CT105 [3DIM3]	*					**	*	

PROJECT	Communication & Digital Lifestyle	Safety & Security	Automotive & Transport	Health and the Ageing Society	Energy Efficiency	Design Technologies	Semiconductor Process & Integration	Equipment, Materials & Manufacturing
CT204 [PASTEUR]			*				***	
CT205 [REFINED]						*	***	
CT206 [UTTERMOST]						*	***	
CT207 [COCOA]						*	**	*
CT208 [REACHING 22]						**	**	
CT209 [RF2T4Z SISOC]	*					*	***	
CT210 [DYNAMIC-ULP]	*					**	*	
CT213 [3DFF]				*	*	*	**	
CT217 [RESIST]			**			***		
CT218 [E450LMDAP]								***
CT301 [EXEPT]								***
CT302 [TOETS]								***
CT305 [SOI 450]								***
CT306 [NGC 450]								***

PROJECT	Communication & Digital Lifestyle	Safety & Security	Automotive & Transport	Health and the Ageing Society	Energy Efficiency	Design Technologies	Semiconductor Process & Integration	Equipment, Materials & Manufacturing
CT312 [MASTER_3D]								***
CT315 [EmPower]			*		**		*	
CT402 [9D-Sense]		*		*		*	**	
CAT120 [CISTERN]	**	*						
CAT121 [EAST]	**				*		*	
CAT209 [H2O]	*	**			*			
CAT406 [NEMADE]				***			*	
CAT601 [SiPoB-3D]						***	*	
CAT801 [TSV-HANDY]							*	***
CAT802 [SAM3]							*	***
CAT408 [NexGen]		*		***			*	
CAT602 [PARADISE]	*		*			***		
CAT311 [TRACE]			***			*	*	

APPENDIX C

Glossary of Terms

AENEAS	Association for European Nanoelectronics Activities
ALD	Atomic Layer Deposition
AMC	Academic Medical Center
ASICs	Application Specific Integrated Circuit
BCC	Body Communication Coupling
BEOL	Back End of the Line
BOM	Bill of Materials
CATRENE	Cluster for Application and Technology Research in Europe on Nanoelectronics
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
CVP	Controller of Variability and Power
DRAM	Dynamic random-access memory
DTC	Design Technology Conference
ECSEL JU	Electronic Component and Systems for European Leadership Joint Undertaking
EDA	Electronic Design Automation
EFEM	Equipment Front End Module
EMC	Electro Magnetic Coupling
EMI	Electro Magnetic Interface
FDSOI	Fully Depleted Silicon on Insulator
FEM	Front End Module
FOUP	Front Opening Unified Pod
FP	Full Proposal

FP7	Seventh Framework Programme
FPGA	Field Programmable Gate Array
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Gbit	Gigabit
Gbps	Gigabit per second
GFLOPS	Giga FLoating-point Operations Per Second
HCD	Hot Carrier Degradation
HID	High-Intensity Discharge
HK/MG	High-K/Metal Gate
HPC	High Performance Computing
HVM	High volume manufacturing
HW	Hard Ware
I/O	Input/Output
IC	Integrated Circuit
ICPMS	Inductively coupled plasma mass spectrometry
IDM	Integrated Device Manufacturer
IGBT	Insulated Gate Bipolar Transistor
IoT	Internet of Things
ISDA	International Semiconductor Development Alliance
LDMOS	Laterally diffused metal oxide semiconductor
LP	Low Power
LPD	Liquid Phase Decomposition
LTE	Long-Term Evolution
LUT	Look-Up Table

MASP	Multi-Annual Strategic Plan
MEMS	Micro-Electro-Mechanical Systems
MIMO	Multiple input, Multiple output
MoL	Middle of the Line
MOOC	Massive On-Line Open Courses
NBTI	Negative Bias Temperature Instability
NFC	Near Field Communication
nm	nanometer
NMOS	N-Channel Mosfet
NVM	Non-Volatile Memory
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PMOS	P-Channel Mosfet
PMR	Professional Mobile Radio
PO	Project Outline
PWP	Per wafer pass
PY	Person Year
QoE	Quality of Experience
QoS	Quality of Service
RDL	Redistribution Layers
RHBD	Radiation Hardening by design
R&D&I	Research, Development and Innovation
RF	Radio Frequency
RFF	Radio Related Functions
RFMEMS	Radio Frequency Micro-electro-mechanical systems
RTL	Register Transfer Level
RTLS	Real-Time Locating System
SDB	Soft breakdown

SDK	Software Development Kit
SEE	Single Event Effects
SEL	Single Event Latchup
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon Germanium
SiP	Systems in Package
SoC	System on a Chip
SOI	Silicon on Insulator
SRAM	Static random-access Memory
SSL	Solid State Lighting
SST	Silicon Storage Technology
STB	Set-top box
SW	Soft Ware
TCO	Total Cost of Ownership
TDDB	Time Dependent Dielectric Breakdown
TEV	Through encapsulant via
TLM	Transaction Level Modelling
TSV	Through-Silicon-Via
USB	Universal Storage Bus
UWB	Ultra Wide Band
VMS	Vision Mission Strategy
VPD	Vapor Phase Decomposition
WiFi	Wireless Fidelity
WLB	Wafer level ball grid array
WLCSP	Wafer level chip scale package
WLP	Wafer level packaging
WP	Work Package