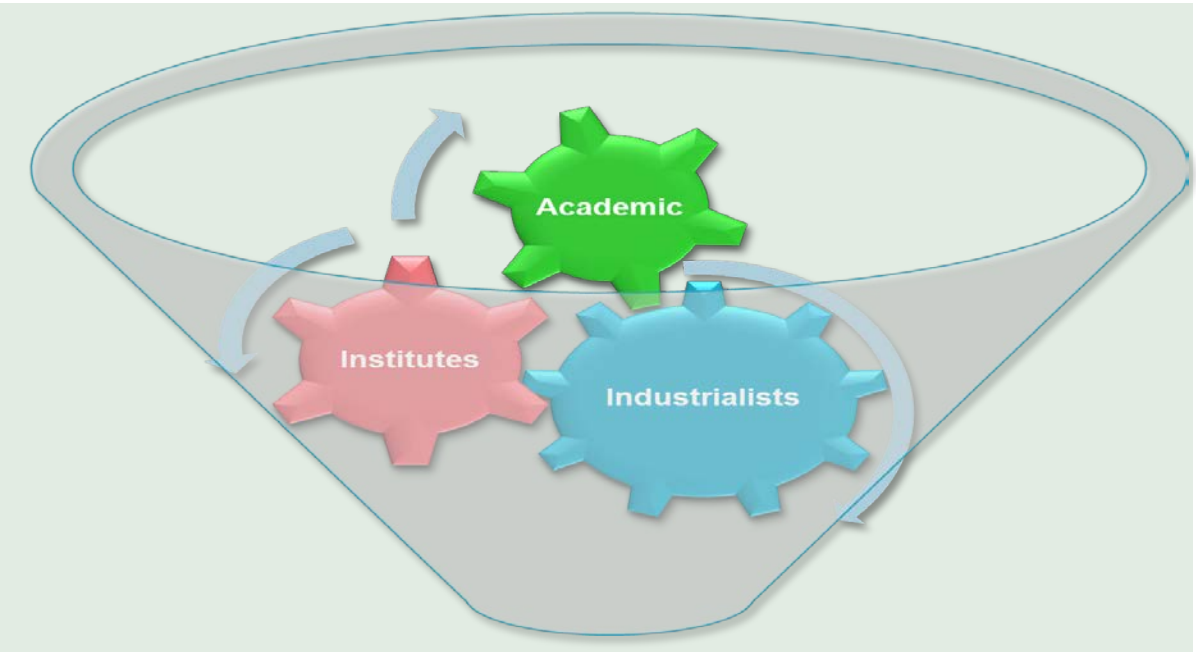
An open European Nanoelectronics Infrastructure for Innovation

Bridging the gap between risk-taking research and innovative technological solutions

Final Report

March 2014



INNOVATION

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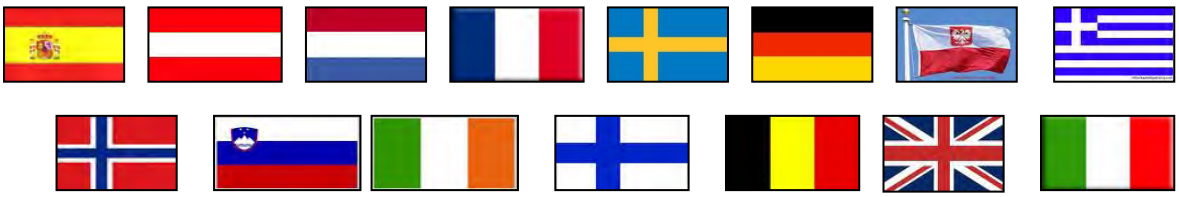
No single Member State has the multi-disciplinary capability to address and sustain the Research & Development & Innovation needed to cover the full value chain and no single company can master all the advanced micro and nanoelectronics technologies necessary to remain competitive. The ENI2 initiative will contribute to structure and coordinate R&D&I in Europe and thereby address fragmentation, avoid unnecessary duplication of effort identify and encourage new or hitherto uncovered areas of technology development and build upon existing and emerging clusters to create a European eco-system 'at the service' of European industry.

ENI2 Core Group

May 2011

ENI2 CORE GROUP

Participant organization name	Country
INSTITUT POLYTECHNIQUE DE GRENOBLE	FRANCE
CONSORZIO NAZIONALE INTERUNIVERSITARIO PER LA NANOELETTRONICA	ITALY
COMMISSARIAT A L ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES	FRANCE
ASM INTERNATIONAL N.V.	THE NETHERLANDS
CIRCUITS MULTI-PROJETS	FRANCE
FRAUNHOFER-GESELLSCHAFT ZUR FOERDERUNG DER ANGEWANDTEN FORSCHUNG E.V	GERMANY
INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	BELGIUM
AIT AUSTRIAN INSTITUTE OF TECHNOLOGY GMBH	AUSTRIA
AGENCIA ESTATAL CONSEJO SUPERIOR DE INVESTIGACIONES CIENTIFICAS	SPAIN
ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	SWITZERLAND
EDACENTRUM GMBH	GERMANY
FORSCHUNGSZENTRUM JUELICH GMBH	GERMANY
ION BEAM SERVICES	FRANCE
CATALAN INSTITUTE OF NANOTECHNOLOGY	SPAIN
INFINEON TECHNOLOGIES AG	GERMANY
INSTYTUT TECHNOLOGII ELEKTRONOWEJ	POLAND
KUNGLIGA TEKNISKA HOEGSKOLAN	SWEEDEN
MICRON SEMICONDUCTOR ITALIA SRL	ITALY
NATIONAL CENTER FOR SCIENTIFIC RESEARCH "DEMOKRITOS"	GREECE
NXP SEMICONDUCTORS BELGIUM NV	BELGIUM
OPEN ENGINEERING	BELGIUM
INSTITUT SINANO ASSOCIATION	FRANCE
STIFTELSEN SINTEF	NORWAY
STMICROELECTRONICS S.A.	FRANCE
STMICROELECTRONICS SRL	ITALY
THALES SA	FRANCE
THYIA TEHNOLOGIJE D.O.O	SLOVENIA
TECHNISCHE UNIVERSITEIT DELFT	THE NETHERLANDS
NEDERLANDSE ORGANISATIE VOOR TOEGEPAST NATUURWETENSCHAPPELIJK ONDERZOEK - TNO	THE NETHERLANDS
UNIVERSITY COLLEGE CORK, NATIONAL UNIVERSITY OF IRELAND, CORK	IRELAND
UNIVERSITE CATHOLIQUE DE LOUVAIN	BELGIUM
UPPSALA UNIVERSITET	SWEDEN
TEKNOLOGIAN TUTKIMUSKESKUS VTT	FINLAND
TECHNISCHE UNIVERSITEIT EINDHOVEN	THE NETHERLANDS
TUBITAK	TURKEY
INSTITUTO DE TELECOMUNICACOES	PORTUGAL



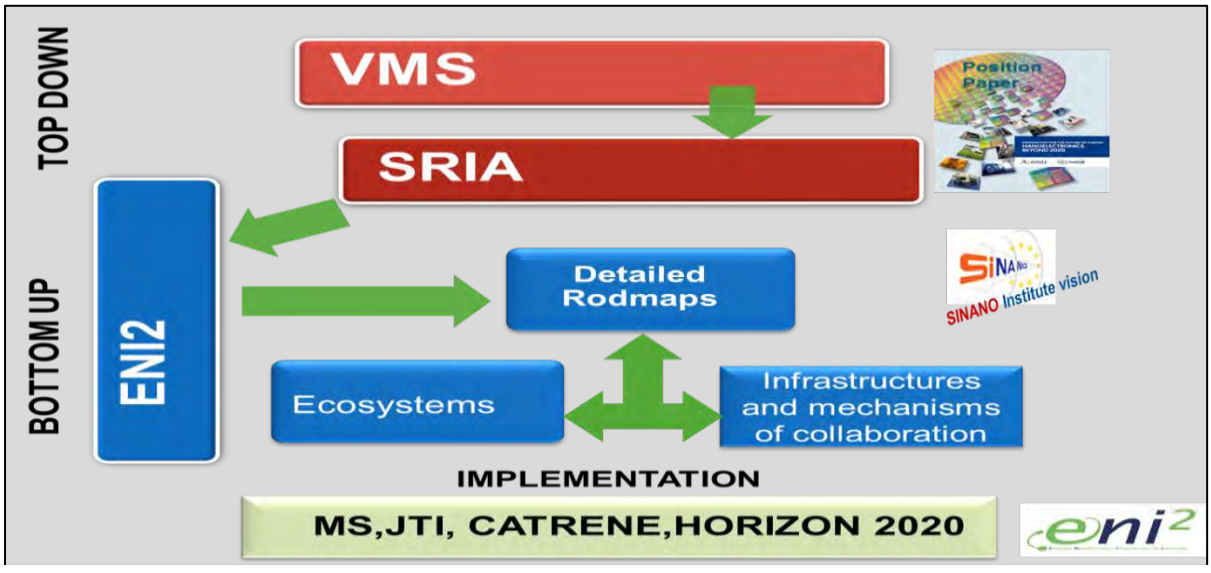
Foreword

This report is built-up together by all the members of the ENI2 Core Group. The members of the Core Group serve on behalf their organization and have a well-recognized expertise in their respective field and a solid experience in European Collaborative Programmes.

1. Executive summary

1.1 Context

The highly-dispersed nature of the nanoelectronics R&D activities in Europe limits the creation of visible effective impact. Europe can be proud to have the global market and manufacturing leaders in advanced CMOS, MEMS, in power semiconductors, security ICs and materials and equipment industry. However, there are no European agglomerations such as Silicon Valley or the Asian foundry companies or well-known economy drivers as kind of global "brand marks" that can act as job creation machines. In nanoelectronics in particular, Europe is suffering from the absence of a global and consistent R&D approach. There is a vital need to identify who the key players are, reinforce alliances between them and organize a new collaborative paradigm to achieve an economic strength based on collimated forces and knowledge. Bundled forces also means, that research based on public funding needs to be more efficient: the research funds used across Europe need to be better coordinated and there needs to be less duplication of work that has no clear justification for being conducted.
In line with the VMS and the SRIA issued by AENEAS and CATRENE and in the context of Horizon 2020 and of the new JTI, the ambition of **The European Nanoelectronics Infrastructure for Innovation (ENI2**) is designed to create mid- and long- term technology roadmaps for cooperative R&D projects in nanoelectronics.



ENI2 members include academia, research institutes, multinationals and SMEs from 15 European countries. ENI2 will help to optimize the efforts, time and funds spent on R&D projects at international level. This will mainly be done by aligning the technological needs and roadmaps for nanoelectronics between industrial and academic partners within a long-term perspective. The ENI2 initiative will also contribute and enhance the possibilities of exploitation of results obtained by research institutes and universities.

The ENI2 Roadmaps will focus on the following 5 areas:

- **Nanoscale FET** (Set Top Box, Smartphones, HPC, mini-servers)
- **Smart Energy** (smart grid, electrical cars).
- **Smart sensors** (Internet of things, e-health).
- **System Design** and **Heterogeneous integration** to offer greater functionality at lower cost.
- Novel semiconductor **equipment and manufacturing processes**.

1.2 Objectives

The collaborative innovation poses four major challenges:

- Development of a vision for collaborative innovation based on the detailed content of R&D&I Programs of European interest,
- Ensuring that the partners are ready to collaborate with each other
- Building trust among partners,
- Defining the respective tasks of the members of the ecosystems and the mechanisms for collaboration.

On the other hand, the key factor of a successful collaborative innovation ecosystem will be based upon the possibility to move from the traditional opportunistic and focused topic calls to flexible and transparent procedures, as already partially started in recent years with the JTI's and PPP's. This will support long term funding support and will create a framework able to transform R&D activities into advanced processes and innovative silicon devices to strengthen European research ecosystems and manufacturing in Europe.

The ENI2 initiative started in 2011 with a core group of partners with the ambition to:

- ***Create the vision***
- ***Build the team***
- ***Define the tasks and individual contribution based on shared understanding of European technology challenges***
- ***Drive the execution***
- ***Install the culture***
- ***Propose long term Programs***

In May 2011 the core group of academic, institutes, and industry experts has issued a position paper with a shared vision, consolidated during sessions in Paris and Brussels. The tasks and individual contributions have been defined in January 2012

and reviewed during several Workshops. To drive the execution and install the culture a working Group, ENI2 has been embedded in AENEAS with the following management structure:

Driving the execution

Role	Company	Name
Project Manager	ST	G.Casanova
Steering Committee	Sinano-Tyndall-FHG-NXP-IFX-ST-IMEC-ITE	F.Balestra-A.Mathewson-J.Pelka-P.Grabiec-W.Dettmann -P.Pype - G.Casanova -A.Van den Bosch
Project Team	Core Group	Annexe
Team Leads	TUDelft-STE-Thales-TUE-ST-NXP-IFX-Sinano-FHG-KTH-CMP-Tyndall-IMEC-	M.Graef-P.Blouet- J.P.N Haagh-G.Thomas-M.Ostling -A.Bouffioux -F.Balestra - J.Pelka- B.Courtois-A.Mathewson - P.Blouet - A.Van den Bosch-
Executive Sponsors	Aeneas office	M.Annergan

Based on the outcomes and assessment of ENI2 acquired during the preliminary phase, it was agreed to focus the work on the:

1) Definition of a strong set of common long term R&D strategic nanoelectronics programs that will stimulate innovation in Europe.
2) Establishment of strategic groupings of research communities with common interests and expertise which will lead to innovation oriented R&D programmes and focus resources on target issues.
3) Definition of the infrastructures and the associate collaborative mechanisms including the:

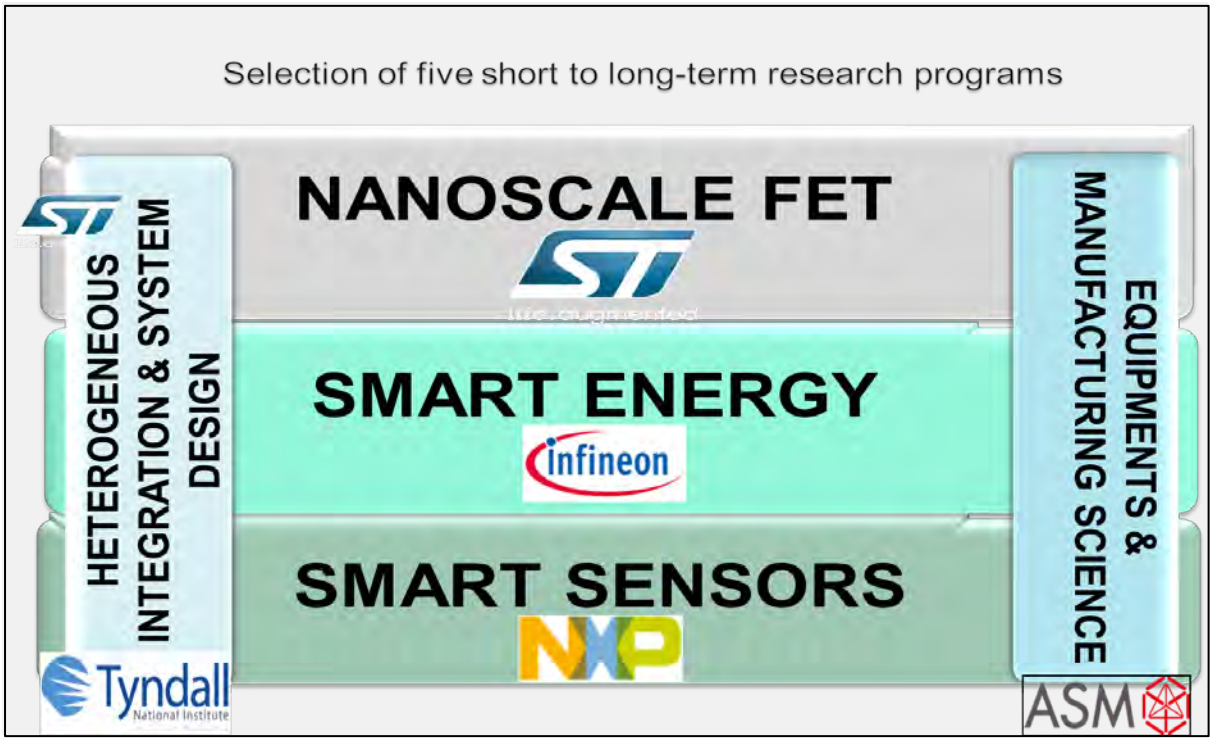
- Structuration of the three levels of the research infrastructure
- Interaction and mechanisms of the collaboration between the three levels
- Definition of European Excellence Centers
- Routes of access for SMEs and Universities to the ENI2 technologies capabilities.

1.3 Methodology

1.3.1 Selection of the R&D nanoelectronics programmes

Five domains have been identified, which cover the need in Europe for manufacturing specialization and product competitiveness in advanced applications, namely **NANOSCALE FET", "SMART ENERGY", "SMART SENSORS", SYSTEM INTEGRATION & HETEROGENEOUS INTEGRATION, MANUFACTURING & SCIENCE**. Within each domain we have identified key projects and research lines based on "short", "medium" and "long" term perspectives.

The rationale behind this concept is that the European Ecosystem must develop a clear vision of the technological priorities to be pursued for each domain and within the different timeframes. For each technological domain, the outcomes will result in the definition of "short-term-projects" (technological development), led by Industrial Partners with Research Institutes and Academia playing a support role, "medium-term-projects" led by Research Institutes with Industry and Academia playing the role of end-user and scientific consultants, respectively, and finally "long-term-projects" led by Academia where Research Institutes and Industry have the role of advisor/steering partners.



1.3.2 Working group

For each of the technological domains, one ENI2 partner is responsible for promoting open discussion among partners around the different topics related to the domain, classifying them within the three time horizons, with the goal to converge on priorities as well as identifying and elaborating *projects*. For the technological domains that have been defined as the main pillars in order to sustain European development in the nanoelectronics area, the objective was to define, map and select the different topics as well as the priorities for the different time horizons (3, 6, 9 years). On Heterogeneous Integration, the objective of the working group (WG) was to place specific attention on the definition of the collaborative activities that will bring added value at European level and, which will contribute to making heterogeneous integration a reality. Concerning the infrastructure domain, the mechanisms associated with the collaboration between the partners and the routes to access of the ENI2 technologies have been identified as the key issue to make the collaboration effective.

1.3.3 Workshops

Several Workshops with many European laboratories have been organized and thorough discussions have been undertaken with the principal players on the European nanoelectronics stage; from academia, to pre-industrial centers up to industry; in order to establish the major structural and technical challenges that face the European nanoelectronics community.

1.3.4 Template

In order to gather all relevant information on R&D priorities as well as the specific expertise resident in each location, the template shown below (e.g. Nanoscale FET) have been filled in by each ENI2 member. This template has also been used for the work devoted to Ecosystem and Research Infrastructures (see Annex).

ENI2 Expression of Interest form

Nanoscale FET **Areas of collaboration**	**Potential contribution Yes/no**	**Priority level (*)**
Properties of materials and devices built at the nanoscale		
Modeling of properties of materials and devices		
Multi-physics and multi-scale modeling methodologies		
Novel materials and new functionalities		
New device architectures		
Novel interconnects architectures		
Development of ultimate processing technologies		
Nano devices for adding new functionalities to CMOS		
Physical and electrical nano characterization		
Integration of very high densities of nano devices		

Other suggested collaboration areas

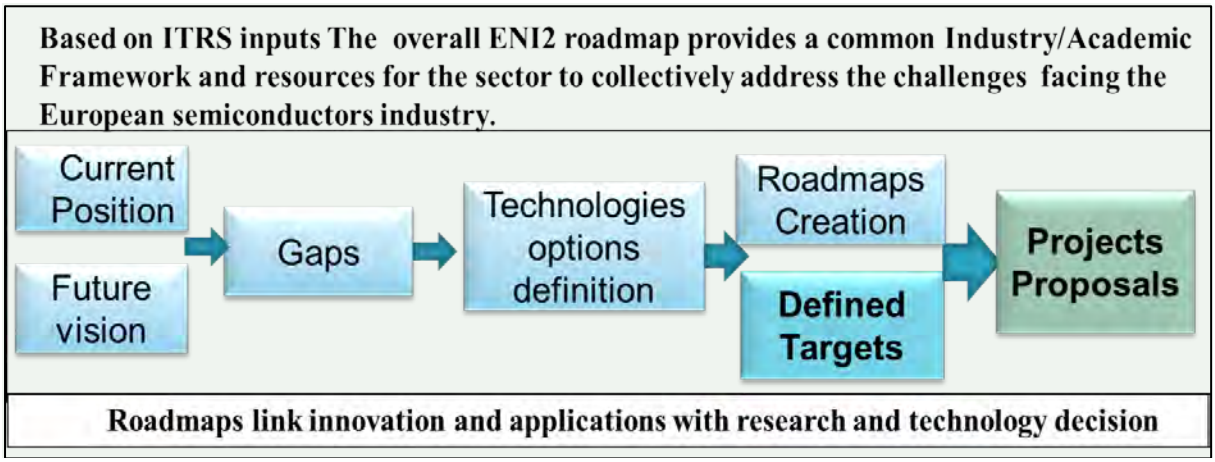
2. Technological roadmaps

The ENI2 Technology road mapping as presented in this report has to be perceived as an effective tool for technology planning and the coordination of efforts at the European level. By capitalizing on the ITRS, the ENI2 road mapping process provides a consolidated and structured consensus view of the future S&T landscape at European level available to decision makers. This technology road mapping has been based on joint, detailed and shared collaborative R&D. The main benefit that it produces is that it identifies the R&D paths to make better technology investment decisions. It does this by identifying critical technologies and technology gaps as well as identifying ways to leverage R&D investments and accelerate the time to market. **This kind of technology road mapping is particularly relevant when different technology options for meeting certain performance objectives need to be pursued.** If there is high uncertainty or risk, different R&D paths may be pursued concurrently. The roadmap identifies precise objectives and helps to focus resources on the critical technologies that are needed to meet those objectives. This focusing is important because it allows the use of R&D resources in the most efficient way. **For the technological domains**

(nanoscale FET, Smart energy and Smart sensors), we have agreed on the following roadmapping process:

- Identify the "Applications" that will be the focus of the roadmap.
- Describe the state of the art and the vision.
- Define the technology options and select the areas of cooperation to be addressed at -European level
- Create the roadmaps by specifying the major technology areas (devices, interconnect, materials…..) and associated targets
- Generate and implement a plan to develop and deploy Long term Programmes.

The figure below illustrates the approach to be taken:



2.1 Nanoscale FET

This domain of the electronic industry is essentially the one that is related to digital technologies (micro components, memories and logic circuits). These devices benefit greatly from a continuous increase in integration density to become obviously smaller but also faster and cheaper. This trend has been developing without abatement for the last 30 years mainly thanks to the MOSFET. CMOS technology is also used for analog chips and for communications chips. However, in this case the MOSFETs are complemented by other active (LDMOS, HBTs…) or passive devices to create the mixed signal class of chip possible. For some time, there has been a consensus that the scaling will end (due to economic or physical reasons) and that BEYOND CMOS devices need to be studied in order to keep working on the reduction of energy consumption of the electronic functions. For memory devices, whose weight in all ICT applications has become increasingly important, the end of the conventional scaling roadmap seems to have already been reached. New architectures and storage mechanisms have to be introduced to satisfy increasing requirements in terms of storage capacity, access speed and low power. With increased transistor density, we have moved from Microelectronics to Nanoelectronics but we are facing a power crisis (especially in battery powered electronics) and power efficiency will become the new Figure of Merit (FoM) for the electronics industry. On the basis of this kind of issue, Nanoelectronics will soon morph into Femtojoule electronics where a stronger emphasis will be placed on power reduction rather than geometry scaling.

2.1.1 Applications needs

The digital IC market based on CMOS technology is evolving from being computer-centric to being focused on mobile platforms. Key application segments in the past were first large computers, then personal computers, which became common in the early 1980s; this phase continued for almost 30 years up until 2009/2010. While personal computers will continue to have volumes of 300M units per year; smart phones have become the next key platform. This trend will be strengthened by the complementary tablet computer, which is a bridge between smart phones and notebook computers. The new multimedia mobile platform volumes will reach 1.5B units in 2015 and will be the most important platform target for IC vendors. The key semiconductor challenge has moved from only performance, to energy efficiency and extreme miniaturisation due to portability and long battery lifetime requirements of mobile computing. One of the main requirements of these systems is the availability of a large storage capability for high quality images, music and videos, based on solid state non-volatile memories. Until now the needs have been satisfied by a combination of DRAM and high density NAND Flash devices, but power constraints are affecting the former, and the latter are close to their scaling limits. **We need to develop and produce state**

CMOS Growth drivers: Cloud infrastructure & Multi-screen clients

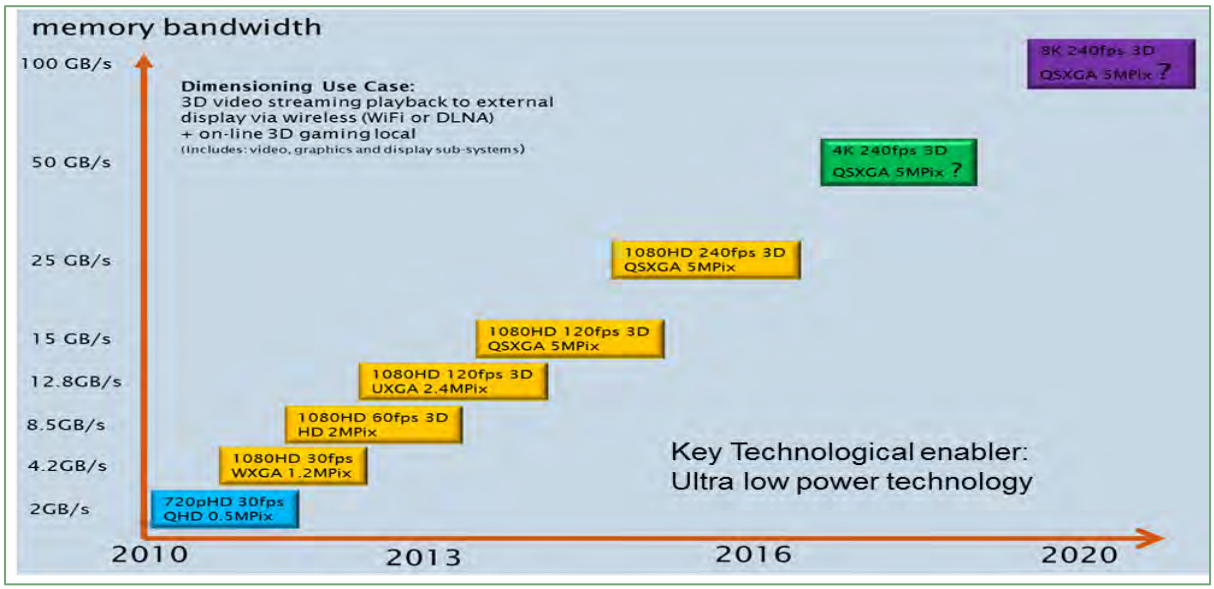
of the art CMOS in Europe that are able to address both the high performance end of the spectrum (3GHz+) and ultra-low power operation in order to serve the emerging multimedia applications and the new mini-servers and HPC markets

Basically application needs are exploding in three main directions generating a huge demand on silicon technologies.

-Multimedia systems

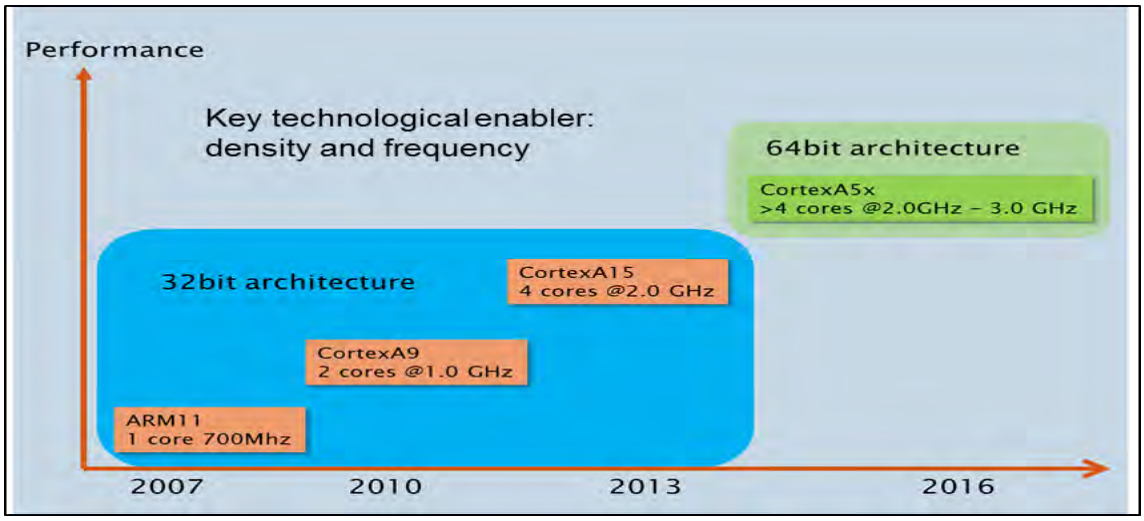
There is an important trend for a continuous increase in terms of resolution and frame rate for multimedia sub-systems. This is a generic trend that is not only visible in the mobile industry. As a consequence, it is exerting strong pressure on memory bandwidth and the processing power needed to process these new data streams especially in the video domain. The graphic below shows the important evolution that has happened in the past few years and what can be foreseen in the future. Even if new codecs like the

H265- HEVC are emerging to limit the file size explosion and maintain a good image quality, this occurs at the price of increased processing complexity which always requires more transistors to implement new functions.



-Processing power

As shown in the figure below, a big change happened in the past ten years on the processor side and even bigger ones are ahead of us. In a few years, we moved from a relatively simple processing node to very complex systems which require very sophisticated memory hierarchy. This has a big impact on the technological complexity in order to sustain the good performance level of the overall computing system while maintaining a very strict control on the energy budget.

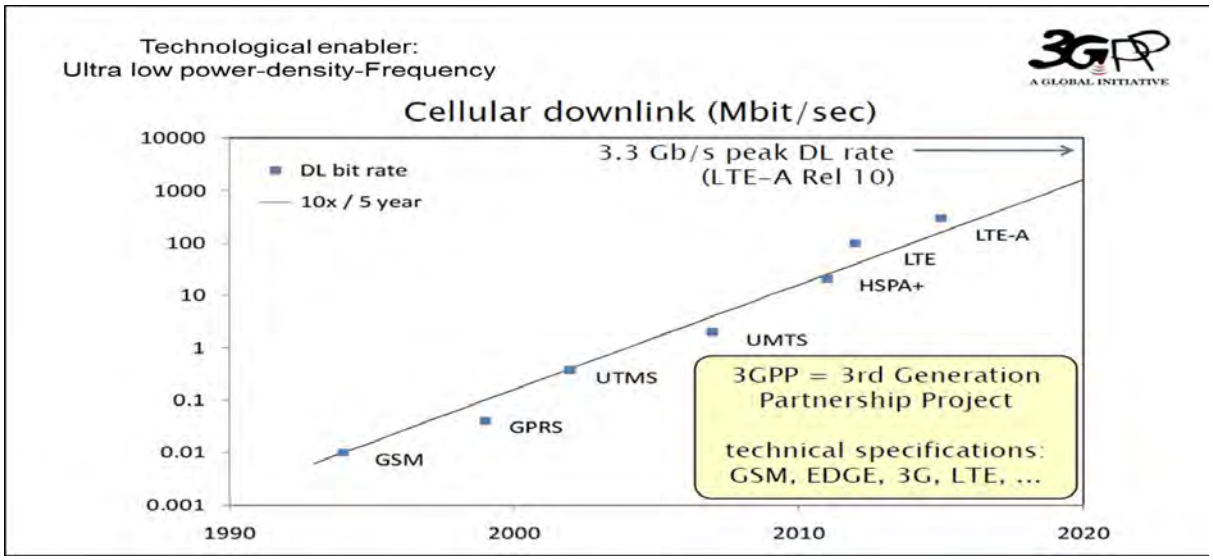


Once again the move from sub-GHz 32bit systems to multi-GHz 64bits systems will generate a tremendous increase in the number of transistors required. This is strongly pushing the technology to provide solutions able to fulfill the needs, but at the same time it is necessary to control the energy consumption to make sure it is still possible to manufacture the new system at reasonable costs.

A proper combination of memory technologies is needed to satisfy the requirements for access speed, memory capacity and power dissipation. New memory technologies like STT MRAM, or resistive switch memories are required to avoid that memory becomes a bottleneck for computing system. A proper allocation of memory types by cache level is required, with an optimized partitioning between memory integrated on-chip, in package or in dedicated high performance storage units (e.g. Solid State Disks).

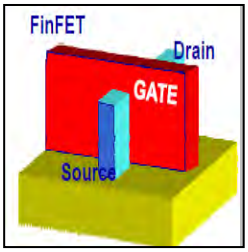
-Communications

In the communication domain, the evolution of the past year and the new trends are also generating a huge demand in processing and power efficiency. This has had a very important impact in a lot of domains because it allows new usage models with connected systems, increased volume of data exchange and this puts substantial pressure on both the client and the server side. This domain also has the requirement for more functions per silicon mm^2 in a more and more constrained energy budget.

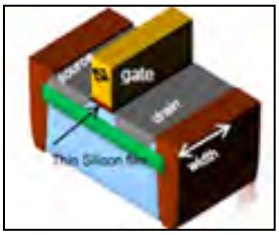


2.1.2 Current position

In production, MOSFETs have achieved the density, of typically, 35 transistors/µ2; making it possible for certain high performance circuits to exceed 1 billion transistors/chip. The minimum feature size printed onto the silicon for those chip is 28



nanometers. At this gate length dimension the conventional planar MOSFET becomes increasingly leaky and new transistor architecture is required. Next generations of technologies (below 28nm) will extensively use FULLY DEPLETED devices which can be implemented in various ways. These kinds of



devices require a very thin film of silicon to operate. **We are entering the domain of thin film technologies** at the same time as operating voltages reach below 1V and optical lithography becomes impractical economically due to the requirement of multiple exposures with complementary masks to print all the features drawn at a given level. Technologies become more complex, and expensive and therefore cost per function cannot decrease as much as it has in the past (cost reach the micro cent/transistor). Going forward, there are **two options that are possible**. We can either continue to drive for transistors with smaller footprint (and feature size) ie:

more transistors per µ2 OR keep maintain feature size constant and stack thin film transistors on top of each other to generate **more transistors per µ3**. Industrially a third option is possible to further decrease the transistor unit cost. In this scenario productivity improvements will be achieved with a leap in economy of scale by processing more chips at the same time, on each wafer (i.e changing the wafer diameter from today's state of the art 300mm to the future proposed standard of 450mm). This will have additional benefits and will require new manufacturing paradigms and equipment. This is an area where Europe is strong but research at this level is very expensive and resources will need to be husbanded very carefully in order to ensure that scaling up the technology platform doesn't diminish the ability to undertake research into device architectures and power reduction scenarios.

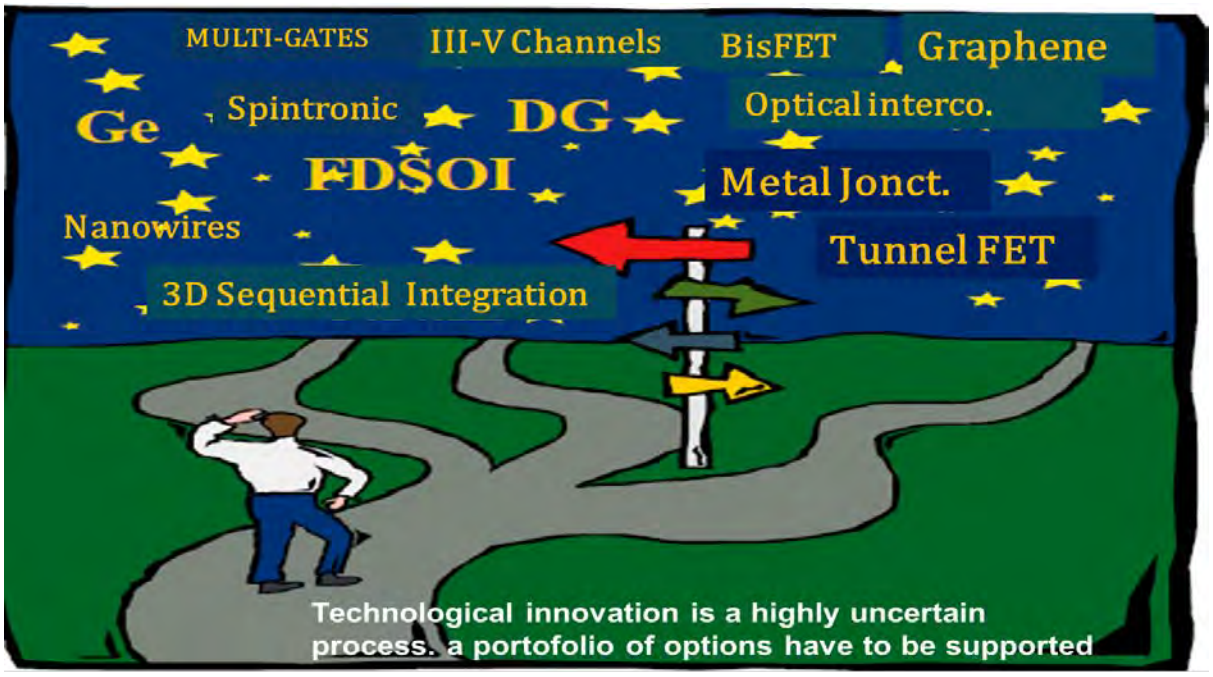
Memories are already now using feature size of around 20nm half-pitch, via double patterning, for NAND Flash, and 30 nm for DRAM. In the former, storage density is further increased by the use of multiple bit/cell. **Stored charge is however reaching it physical limits,** and no cost effective lithographic techniques is available to go below 20nm. **Going forward will require developing new memory technologies that are independent from charge storage**, like magnetic or resistive memories, and reducing cell footprint, and dependence on lithography by introducing vertical architectures. Low voltage memory technology is also required to integrate large quantity of non-volatile memory in advanced CMOS architectures, as required for microcontrollers used in most industrial and mobile applications.

The international investigations for Ultimate CMOS and beyond-CMOS are covering the followings domains:

- **Implementation of advanced multi-gate structures for ultimate CMOS**. The challenges deal with the fabrication of advanced planar and non-planar multi-gate (common or independent gates) MOSFETs to 10 nm gate length and below, the control of short-channel effects, the control of threshold voltage and leakage currents, source/drain engineering to reduce parasitic resistance for thin film fully depleted (FD SOI) or fully inverted (FinFET, GAA…) devices, strain enhanced velocity and ballistic transport and alternative Ge/III-V channel materials and the use of substrate and channel orientation, and the improvement of the reliability of novel devices, structures, and materials with the control their failure mechanisms.
The reduction of sub threshold current and sub threshold slope, and the associate Vdd and power scaling, is of tremendous importance.

-**In the charge-based/FET Beyond-CMOS field**, which could extend CMOS scaling and/or performance (ultra-low power, new functionalities,…), the following Nanoscale FETs will be investigated: Nanowire FET, Tunnel FET, CNT FET, Graphene Nanoribbon or other 2D layers (MoS2, Silicene…) FETs. Other candidates are Negative gate capacitance FET, SpinFET, IMOS, Atomic switch, and Mott FET. For memories: vertical stacking of Flash cells, zero capacitor DRAM.

-**In the non-charge-based, non-FET Beyond-CMOS devices**, the possible candidates are NEMS switch, Spin wave devices, Nano magnetic Logic, Excitonic Field Effect Transistor, BiSFET, Spin Torque Majority Logic Gate, and All Spin Logic. For memories: magnetic memories, based on the Spin Transfer Torque effect (possibly thermally assisted), resistive switching memories like PCRAM and RRAM.

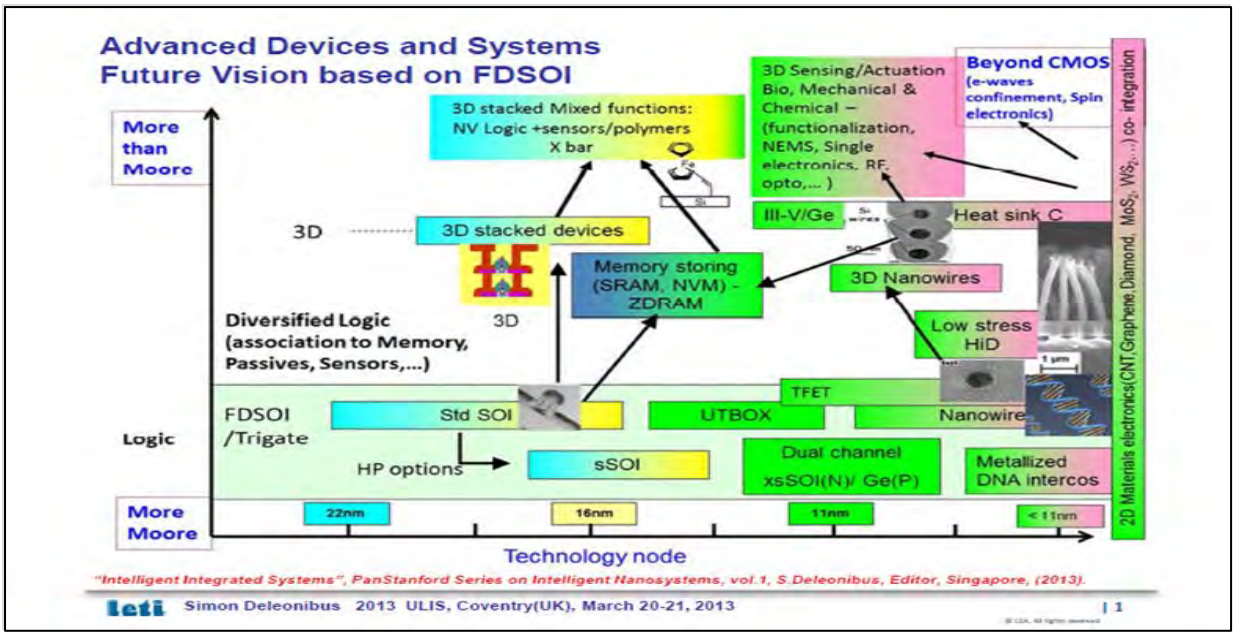


Concerning ultimate processing, the main investigations will deal with the continued scaling of SOI/multigate device (EOT, junctions, Si film, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation…),. It will also see the introduction of high mobility channels (based on III-V and Ge) to replace strained Si, the EOT scaling below 0.7 nm with appropriate metal gates as well as the achievement of clean surfaces which are free of killer defects, and the introduction of 450mm wafers.
With regard to lithography, EUV remains the leading candidate for 1X node and below, multiple patterning with EUV or reducing the EUV wavelength to 6 nm could also become options for the future. Alternative technologies are mask less E-beam lithography, Imprint, or direct self-assembly using the bottom-up approach for the very long term options .

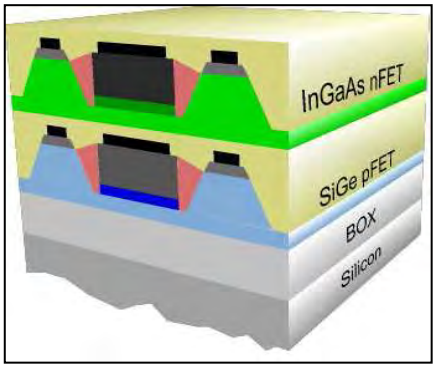
With respect to novel interconnect architectures, researches are to be devoted to ultra-low-κ materials with κ<2.0 and to introduce air-gaps, with a hybrid of low-κ materials and air-gaps possibly being the best solution. TSV and 3D stacking technologies will also become of key importance.
In order to replace Cu, other metals (Ag, silicides …), Nanowires, CNT, Graphene Nanoribbons, Topological insulators, Superconductors, and novel non-charge-based interconnects (Optical -interchip/intrachip, or Wireless), will need to be investigated.

2.1.3 Future vision

Issued from collaborative research at European level, a promising way to implement FULLY DEPLETED devices is through the **use of a thin film of silicon on top of insulator layer**: this technology using SOI substrate is called **FDSOI**. FDSOI can produce planar quasi double gate devices while a further option can be to use a thin vertical film of silicon (called fin) surrounded by the gate stack on 3 sides. This latter architecture is called a FINFET by some and a TRIGATE by others. The FINFET/TRIGATE architecture can also be built (with added advantages) on a SOI substrate or on Bulk.



At 14nm and possibly at 10nm the 2 architectures (planar (2D) FDSOI and 3D FINFET) will compete and will probably address different parts of the power spectrum (HP vs LP technologies). However, this trend towards thin film transistors could become a way to stack active transistor layers using the wafer bonding technique. It is envisioned to be able to stack multiple thin semiconductor films addressing the performance need of N and P type transistors (films could be of compound semiconductor materials or even single layer 2D crystals like graphene or MoS2). The sequential stacking of transistors inside the same chip constitutes a monolithic 3D integration and it can be coupled to a 3D stacking of heterogeneous chips together by the 3D TSV technique. Ultimately, we foresee the possible combination of a 3D transistor architecture within a given semiconductor layer, a sequential layering of active films creating a 3D monolithic chip, and the 3D stacking of chips onto each other using TSV to interconnect them. The whole thing will create a highly compact electronic system.



For memories, the development of low power cross-point RRAM cell, will allow the stacking of several memory layers on the same CMOS substrate, thus allowing very high density memory architectures.

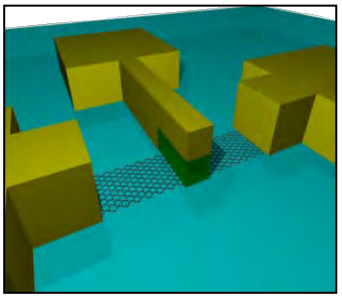
In the future, we will need to be less concerned about more transistors per mm2 and we will need to consider using more transistors per mm3 or more functions per mm3 as a metric. We need to think 3D More MOORE and 3D More Than MOORE (using as much as possible existing infrastructure). Stackable Transistor architectures would be preferred.

There are two ways to make a mixed technology three dimensional system:

- ***By STACKING active semiconductor layers*** within the same chip by some form of deposition or epitaxial approach where channel material would be the variable that would improve the performance

-By STACKING heterogeneous chips onto each other and connecting by 3D vias called TSV (Through Silicon Vias).

Those two techniques are additive and a full system is envisioned (like an autonomous "zero power" system for the Internet of Things).



For long term Beyond-CMOS options, which could be integrated on CMOS platforms, the **most promising solutions are the following**:
Multi-gates sSi, Ge or III-V Nanowires ; Heterogeneous Ultra-thin-body Multi-gates Tunnel FET, Fe Gate FET, NEMS and Spintronics for Ultra-low-power ; Graphene or other 2D layer (MoS2, Silicene,…), CNT channel MOSFETs and Tunnel FETs ; Controlled assembly of nanodevices or combined top-down and bottom-up approaches for Nanowires and CNTs.

2.1.4 Areas of Cooperation

To remain at the forefront of state of the art for miniaturization and integration of nanoelectronic devices while dramatically increasing their functionalities, a coordinated European research effort is required in the following fields (including supporting fields):

- **Basic understanding** of the physical, chemical and electrical and magnetic properties **of materials and devices built at the nanoscale**. Modelling of the properties and devices from ab-initio models for deposition of material layers to compact electrical model in devices.

- **Multi-physics and multi-scale modelling methodologies** (e.g. first principle simulation for band structure, quantum transport, multi-sub band Monte Carlo, compact models including quantum and atomic scale effects, thermo-optical-electro-mechanical effects) for Nanoscale FETs used in future MM and MtM applications.

- **In-depth study of novel materials** with adapted behaviour and processes for high performance nanoFETs and new functionalities (e.g. passive and active components for RF applications, Optoelectronics). Examples where a strong effort is needed are alternative and uniaxial/biaxial strained channels (including Ge and strained Ge, III-V on Si, various orientations), Schottky barriers with dopant segregation techniques for source/drain, novel gate stack materials which go beyond Hf-based dielectrics, materials to improve interconnections of transistors.
- **In-depth study of novel materials** with adapted behaviour and processes **for high performance memory technologies** not based on charge-storage (e.g. magnetic materials, resistive switching materials, interface and isolation layers). These materials can be used also for the development of artificial synapses for neuromorphic computing architectures.

- **Novel interconnect architectures**, e.g. Optical interconnects as well as intra- and inter-chip wireless interconnections, which could overcome the limitations of the traditional metallic interconnects.

- **New device architectures for ultra-low power, high performance and memory or embedded memory applications,** e.g. (independent) Multi-gate/Multi-channel MOSFETs, Tunnel FETs using ultra-thin films/alternative channel materials/multi-gates/1D structures, Si/Ge junction less and 3D integration of Nanowire FETs, Universal Memories combining volatile and non-volatile functions and usable for embedded memory applications.

- To be comprehensive**, new device architecture studies must include all aspects of their insertion into the technology platform;** such as impact on the design of elementary functions, compatibility with the design flow, variability in the manufacturing environment, testability of products, as well as intrinsic reliability under stress conditions.

- **Nano devices for adding functionalities to CMOS**, e.g. Nanowires for Nano sensing (thanks to the huge increase of its surface-to-volume ratio constitutes an ideal elementary block for highly sensitive sensors), Photovoltaic or Thermoelectric eenergy harvesting, or RF applications.

- **Physical** (e.g. roughness, dimensions, strain, dopant imaging, composition and density) and electrical (e.g. multiple interfaces and channels, surface states, transport, contacts, single impurity, variability/reliability, new physical mechanisms in very small volumes) **nano-characterization of nanoscale FETs**. Without those nano-characterization techniques it becomes impossible to ensure control and repeatability over the processing.Integration of very high densities of nanodevices by combining the top-down and bottom-up approaches using CMOS compatible technology.

- **3D Sequential Integration**: 3D integration is currently under great investigation because it offers a solution to continue to increase transistor density while relaxing the constraint on the transistor's dimension and it eases the co integration of highly heterogeneous technologies in comparison with a planar scheme. 3D sequential integration offers the possibility of using the third-dimension potential: two stacked layers can be connected at the transistor scale. This contrasts with 3D parallel integration, which is limited to connecting blocks of a few thousand transistors.

- **Development of ultimate processing technologies** (e.g. EUV lithography, multi-ebeam lithography, Nanoimprint, Atomic layer Deposition, Plasma ion Implantation, etc…) As well as next generation wafer size - 450mm – for the advanced technology nodes.

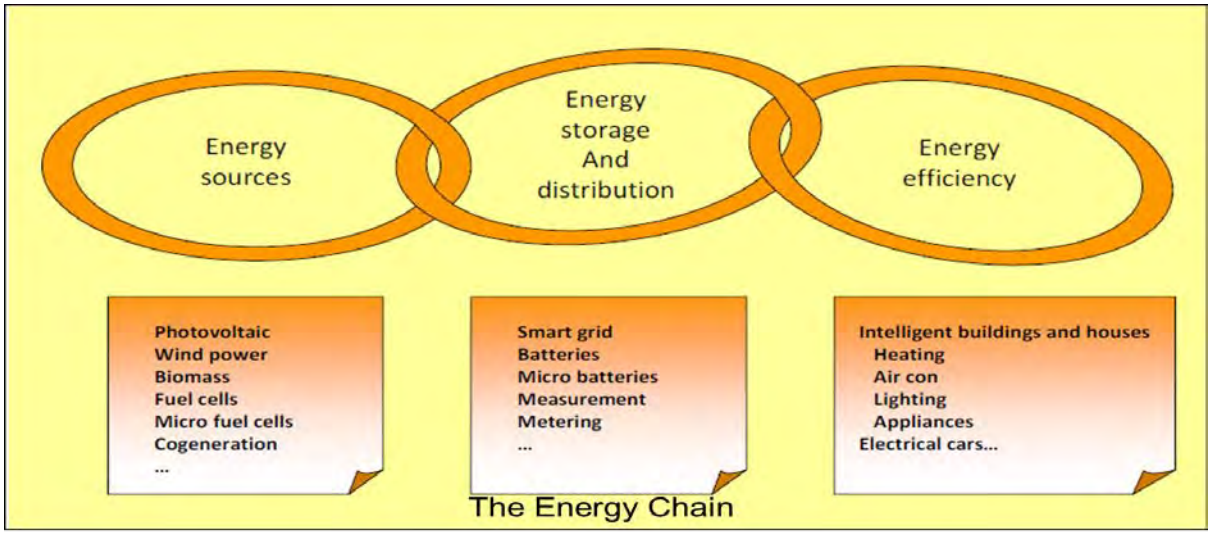
2.1.5 Roadmaps

	2014	2017	2020	2023
ULTIMATE CMOS	-**CMOS:** 2nd gener. high k/metal; Si+stress; S-D engineering; FD-SOI: Variability /Reliability Transport mechanisms (VRTM)	Next generation highK metal K>30 E0I<0,7/0,8nm. Strained Si or alternative Channel on SiGe IIIV-Advanced S-D architecture –VDD scaling, VRTM short channel leakage model and characterization 1st principle simulation/quantum MSB MC simulations- Modeling interconnectsof chemical thermomechanical and electrical properties of new materials	MG structure- 10nm MOSFET and below, control of SC effects, TV and LC, source drain engineering to reduce parasitic resistance for FDSOI or FinFET, GAA.., devices, and alternative Ge/III-V channel of novel devices, structures and the use of substrate and channel orientation-failure control mechanisms
BEYOND CMOS	Nano wires bAssesment	Carbon-based (Graphene,CNT, FETs nanoelectronics with: - high on-off ratio co-integrated with high k dielectric and low resistance contacts-Control of CNT properties,bandgap distribution and metallic fraction	Multi-gates sSi, Ge or III-V Nanowires ; Heterogeneous Ultra-thin-body Multi-gates Tunnel FET, Spintronics r ; Graphene or other 2D layer (MoS2, Silicene,…), CNT channel MOSFETs and Tunnel FETs ; Controlled assembly of nanodevices or combined top-down and bottom-up approaches for Nanowires and CNTs.*
NOVEL INTERCONNECT ARCHITECTURE	-New materials to meet conductivity requirements and reduce the dielectric permittivity -Electrical, thermal, and mechanical reliability -Three-dimensional control of interconnect features with it's associated metrology -Modeling and characterization	-Low-κ dual damascene metal structures / air gap-Optical and RF interconnects, CNT/Graphene interconnects/via -Identify solutions which address 3D structures and other packaging issues -Modeling/characterization for new interconnects	Ultra low-κ materials with κ<2.0 and to introduce air-gaps, the hybrid of low-κ materials and air-gaps could be the best solution. The TSV and 3D stacking technologies will also become of key importance.In order to replace Cu, other metals (Ag, silicides, …), Nanowires, CNT, Graphene Nanoribbons,Topological insulators, Superconductors, and novel non-charge-based interconnects (Optical - interchip/intrachip, or Wireless
ULTIMATE PROCESSING	-Double and multiple patterning -EUV lithography -Atomic layer Deposition, MBE/MOCVD, High aspect ratio dry etching, Plasma ion implantation, Plasma enhancement PLD, Epi growth --Front-end process model. and phys. /electr. characterization for nm structure	EUV lithography/extendibility : *Higher source power *Possible double patterning *Possibly new resist -193 nm immersion multiple patterning -Multi ebeams Maskless lithography / Imprint lithography -450 mm wafers	Continued scaling of SOI/multigate device (EOT, junctions, Si film, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation…), High mobility channels (based on III-V and Ge) to replace strained Si, the EOT scaling below 0.7 nm with appropriate metal gates, introduction of 450mm wafers. Multiple patterning with EUV Maskless-E-beam-Imprint, or Direct self assembly using the bottom-up approach for very long term.

3D SEQUENTIAL INTEGRATION	Thermal budget management. Electrical contacts/silicidation. Cleaning and surface preparation Intra-layer interconnects	Strained and/or orientation optimised materials on each level. N/P over P/N and/or CMOS/CMOS solutions. Co-integration with resistive memories within interconnect and in intra-layer Interconnects schemes. Mix 3D and TSV for system solutions	New high mobility materials. Extension to three or more device layers. Vertical structures. Interconnection congestion management. Deep field of focus litho (e-beam) Photon/electron sensitive materials for litho
MEMORY ARCHITECTURES	Charge storage: - vertical cell architectures, - new capacitor materials for DRAM Non-charge storage: - STT memories, - multilevel PCM memories, - cross-point RRAM	Non charge storage: Higher density MRAM memories,Multi-layer, multi-bit RRAM memories	Non charge storage: - 3D integration of different memory architectures; - molecular memories

2.2 Smart Energy

The "Smart Energy" terminology has been defined for nanoelectronics solutions dedicated to all energy-related applications and markets. Covered under this umbrella are **technologies, materials, integration methodologies and processes for the realization of more energy efficient devices and systems.** Technologies combining the integration of power semiconductors with "smart" feature capabilities and new materials, in order to provide high efficient all-in-one "power", in System-on-Chip (SoC) or System-in-Package (SiP) forms are addressed. "Smart Energy" also covers the market introduction and penetration of **a new class of power devices based on wide band gap semiconductors such as SiC, GaN or AlN.** Strengthening the European research and innovation infrastructure in these areas will enable Europe to be a leading provider for all kind of solutions dealing with the intelligent use, generation and distribution of energy, in particular: Renewable Energy, Intelligent Buildings, Smart Grid, Electrical



Vehicles.

Being an "open innovation" circle, new topics brought in by the partners and evolved from the discussion amongst the partners will be covered. The objective will be to create a clear understanding regarding a sustainable roadmap for the different smart energy related technologies, the needs for a collaborative development set-up and a

clear identification of the win – win opportunities of cross-border partner collaborations.

Changes are always fundamental for success and leadership. **The emerging European market in this sector is huge, and the room for new "Smart Energy" solutions and associated enabling semiconductor technologies is correspondingly large.** Strengthening the European research and innovation infrastructure in this area will enable Europe to be a leading provider of all kind of solutions dealing with the intelligent use, generation and distribution of energy.
The world in the 21st century has to cope with growing worldwide population, limited conventional energy resources, climate changes and the need to reduce CO_2 emissions. All this is challenged by the wish of the individual persons to reach, keep or even improve their European lifestyle. Highly efficient and intelligent use of energy is a key enabler to solve these socio economic challenges. The yearly market growth rate for energy related semiconductors is expected to be above 10% and new applications are, from a global perspective at the beginning of their success story.
The "Smart Energy" battle is now very engaged at a worldwide level and represents a true challenge. Such a high level cooperation as is planned within ENI2 is necessary in order to achieve the whole R&D and production cycle to the benefit to the overall European society. The full know-how and process chain (starting from raw wafer materials up to the end-products) must be addressed.

2.2.1 Applications needs

-Energy sources

- DC/AC converters for solar power, AC/AC converters for Wind power: modules, switches, diodes, ICs supporting highest energy efficiency in power conversion
- Panel switch: intelligent switch for individual control of photovoltaic solar panels, and communication ICs.
- Smart "Sun tracking": intelligent motor control for orientation of photovoltaic solar panels (+30%)

-Energy storage and distribution

- High voltage smart switches for grid coupling and energy transport in AC/DC/DC/AC for HVDC (High Voltage Direct Current)
- Smart grid monolithic AC switch with high galvanic isolation, very low R_{on}, self-powered, over current, voltage, temperature protected, full control and status indication, communication
- Smart meters with contractual electricity consumption measurement and communication features.
- Power switches for energy crossroads and routers for individual energy sources Management
- DC- DC converters for direct DC use from wind or photovoltaic sources in the connected neighborhood (retail houses, manufacturing sides, office/large buildings)
- Highly efficient converters for all kind of bi-directional energy flow for intermediate storage applications

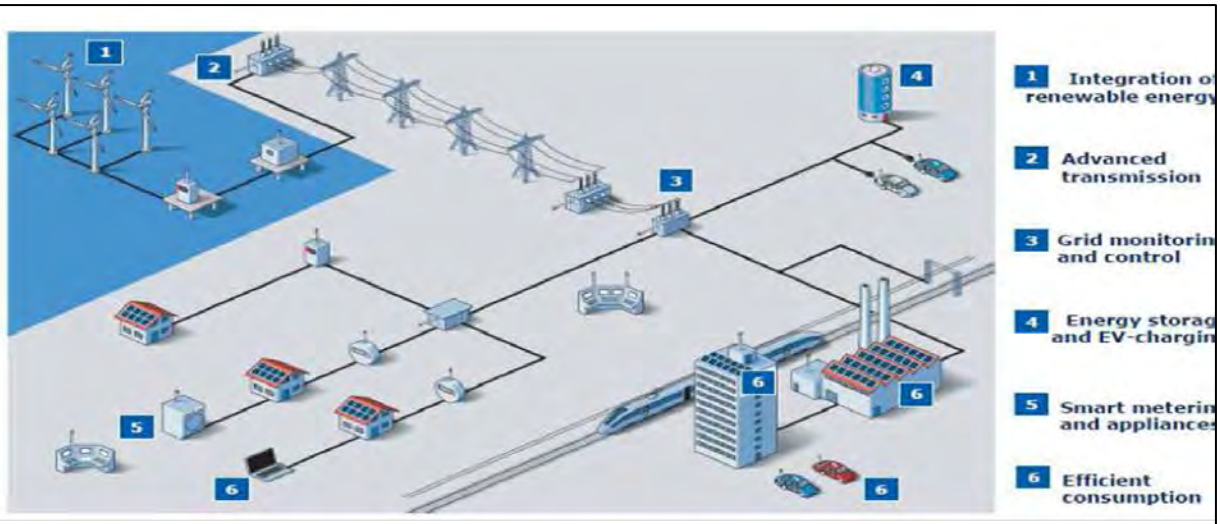


Fig 1 : Entire Energy "food chain" from generation via distribution to consumption, in all segments semiconductors, power technology devices are required (source:Infineon)

-Energy efficiency

Intelligent Buildings

- Energy scavenging systems (temperature/light/vibrations) for self-powered sensors: a very generic architecture including energy sensor, thin film micro battery for storage, power management IC, building parameter sensor (temperature, pressure, humidity, light, windows and doors position, chemicals, air quality, human presence, human activity…), data recording and computing, and full communication features (RF)
- Lighting applications
- Smart plugs
- Smart energy breakers

-Electric cars (e-cars)

- Power switching modules in motor drive inverters
- Battery management and reverse protection
- Energy braking recovery system
- High power traction

-Substitutions of mechanical or hydraulic systems

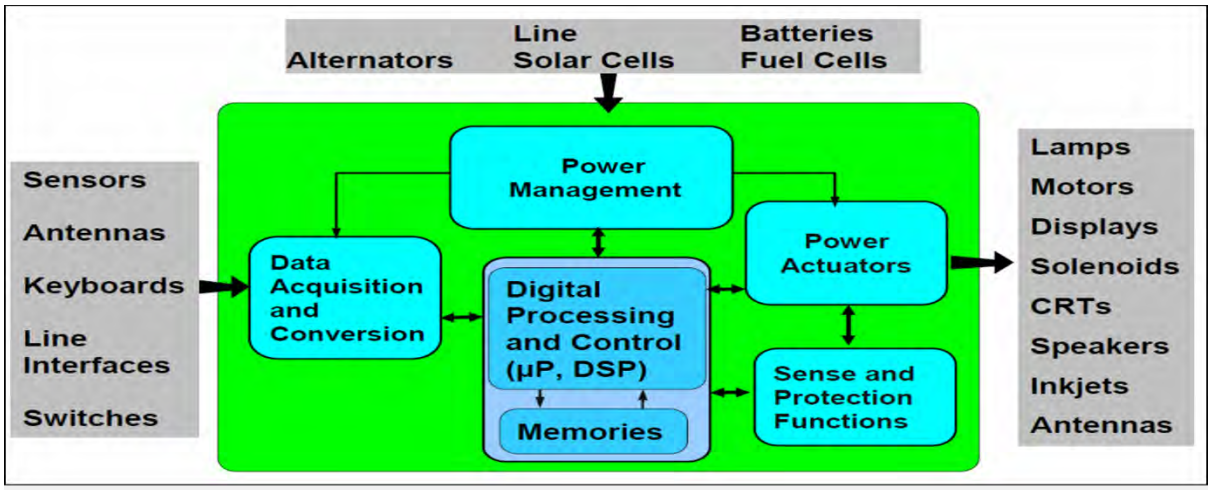
- DC bus systems with intelligent controllers and switches
- Electric drivetrains in conventional applications

2.2.2 Current position

In "low-medium voltage", and due to the good performance of silicon in this range, "**Up-to-150V Smart Power" is continuing to take profit from the silicon mainstream** in terms of fundamental operations, i.e. lithography, implantation and CMP. Silicon CMOS-based Smart power ICs will continue to address new challenges into the coming energy-related applications, and can take benefits from both "More Moore" (MM) and "More than Moore" (MtM) results to be achieved on silicon during the coming years. **Above 150V** and definitely beyond 600V, i.e. for alternative energy markets, intelligent buildings, smart grid, electrical cars and more… **silicon still offers room to improve its performances** and it will do so, especially looking at improving MOS-IGBT-JFET switches.

2.2.3 Future vision

New "wide band gap semiconductor materials" are much more promising in offering higher performant switching cells composed of Schottky diodes plus MOS-IGBT-JFET switches. **Gallium Nitride (GaN) and Silicon Carbide (SiC) offer better voltage** (100V/µm instead of 10V/µm in silicon) and much higher temperature operation (200°C instead of 125°C). Although these materials are very interesting, **they require the development and control of new processes** like homo epitaxy, hetero epitaxy on silicon, localized epitaxy, and also the design of very new device architectures. Diamond, as the Holy Grail to conquer, would offer 1000V/µm and as well as definitively the best class in term of heat dissipation. These new semiconductor materials with higher junction temperatures will ultimately lead to **new challenges and research for the integration into packages, for bonding and for the connection to heat dissipation systems.**



Generic architecture of a "Smart energy" product

The "Smart" side which brings intelligence and numerous added features to the "Energy" side is typically using "very low voltage" (a few volts) and it may also require new materials in the "More Moore" and "More than Moore" challenges (CMOS, Ultimate CMOS, beyond CMOS, Heterogeneous/3D integration and packaging). In addition, **all these derivatives have to be compatible with a "Power" environment** and consequently they may have to be made for their operating conditions e.g. it might be necessary to investigate(DSP core, CPU or memory immunity during an high current switching operation with the additional complexity of adding operation at high junction temperatures).

Integration of "Smart" and "Power" will be achieved either under single-chip form (when materials and processes are compatible) or 2D/3D multi-chip combination, always looking at optimizing global performance-to-cost ratio.

2.2.4 Areas of Cooperation

Overall picture: ENI2 is an initiative from core partners within the European semiconductor community. A solid top level base has been set by the AENEAS AWP for future research activities. For the „smart energy„ domain the relevant topic in the AWP is the chapter on Energy Efficiency including the specific Grand Challenges and the dedicated topics within the chapters Design Technology, Semiconductor Process and Integration and Equipment, Materials and Manufacturing.

- ***Materials and associated processes***

- In addition to silicon (10V/µm), new materials dedicated to "Power" are necessary, along with a road map going through Silicon Carbide and Gallium Nitride (100V/µm), and then ultimately to Diamond (1000V/µm). New materials and structures for voltage isolation are also a key issue. The associated manufacturing processes must be widely developed, with a specific focus on epitaxy (homo epitaxy, hetero epitaxy on silicon, localized epitaxy) because traditional implantation and doping processes are inefficient and difficult to achieve for these new materials. Processes must be compatible with mass production, cost objectives and further integration into appropriate packaging. The reliability aspects have to be considered on top, since the typical automotive domain applications are in long term usage as in infrastructure elements or for the use within the automotive domain.

- New materials dedicated to the "Smart" side are necessary in order to bring derivatives outside the CMOS mainstream. For instance, sensors, micro supply, micro energy sources and micro batteries, transformers, transducers, and integrated passives represent high added value to energy-related "Smart energy" products. These devices must be compatible with further integration.

- However, in addition to semiconductors, two main challenges have to be solved to leverage the full benefit of advanced innovative semiconductors for "smart energy" and it is important to acknowledge these and anticipate the upcoming requirements. These are;

- New materials, dedicated to improve large value capacitors and inductors used in power conversion architectures, and high temperature capable package and integration technologies have to be developed to cope with the capabilities of the new materials for semiconductors.

- **Architectures**

Whatever the materials, new architectures are also necessary to allow higher "Power" performance, and among them, 3D is a key issue. This is true on the electrical, thermal, magnetic, and mechanical aspects.
"Smarter" and "Smarter" chips are being requested, to handle future complex systems solutions allowing full control, complex data storing and computing, with automatic sensing and instantaneous status feedback etc.. ….

- **Simulation Tools**

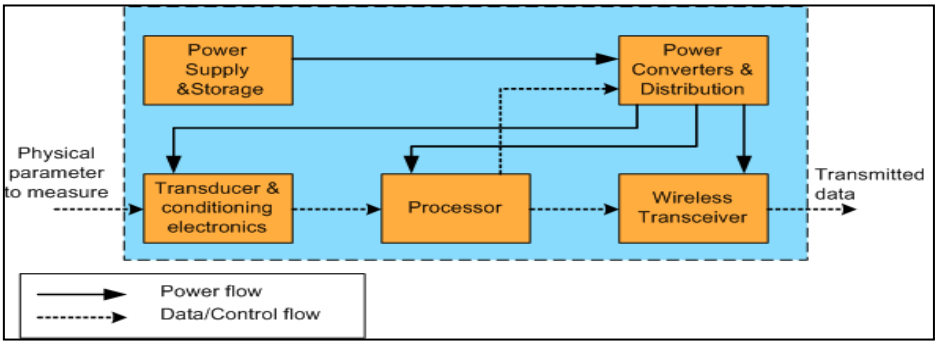
State-of-the-art simulation tools are today dedicated either to electrical, mechanical, thermal, optical or magnetic strength fields. Some tools have started to offer a mixture of the different domains but, for "Smart Energy", very significant improvements still remain necessary to achieve in order to simulate the true physical material and behavior of architectures, required to reduce development cycle times and costs.

2.2.5 Roadmaps

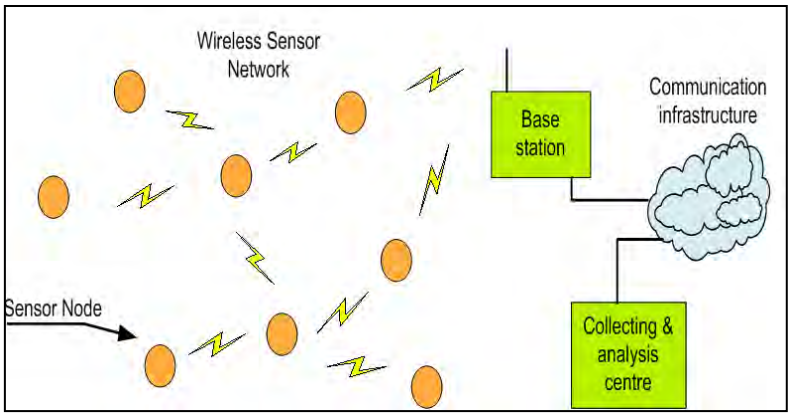
	2014	2017	2020	2023
1. COMPOUND MATERIALS / New Materials	-SiC -III-V materials knowledge from CMOS to power -Materials for capacitors, inductors -Growth of GaN in comb. with high k. -MIM devices for RF -Carbon Based Graphene Nanoelectronics Technologies : ft .5THz	-GaN -On SOI med. Power -New materials and associated processes for Smart derivatives compatible with power -High power GaN devices suitable for PV applications -GaN/Si tandem PV cells -MIM devices for RF	-Sapphire, Diamond -New materials and associated processes for Smart derivatives compatible with power -Piezo NEMs for energy harvesting; Thermoelectric nanodevices; -RF and THz energy scavenging based on TFT and MIM antennas -Carbon Based Graphene Nanoelectronics Technologies: ft higher than 1THz	
2. INTEGRATION OF SMART AND POWER	-Sensors, logic, etc. with power Integration -technologies for energy harvesters	-Sensors, logic, etc. with power -Energy harvesters	-Energy harvesters	
3. PACKAGING	-Hot spot resistant packages	-New 3D power semic. Architecture -Hot spot resistant packages	-Hot spot resistant packages, connections, …	
4. PROCESSING	-SiC >1kV -GaN on Si -Low power mixed signal & RF -Logic with HV applications -300mm power producton technology -Material deposition – e.g. Laser, spray, sputter, ALD and characterisation of ultra-thin dielectric multi-layers	-SiC >1kV -GaN on Si -Low power mixed signal & RF -Logic with HV applications -300mm power production technology -Material deposition processes and characterization of ultra thin layers	-Diamond -Saphire -Material deposition processes and characterization of ultra thin layers	

2.3 Smart Sensors

A smart sensor is made of a measurement chain composed of a sensor (also called transducer that transforms the sensed parameter into an electrical signal), some analogue conditioning electronics, a processor and a wireless transceiver as well as a power distribution chain composed of a battery or energy scavenger and of a power management unit.

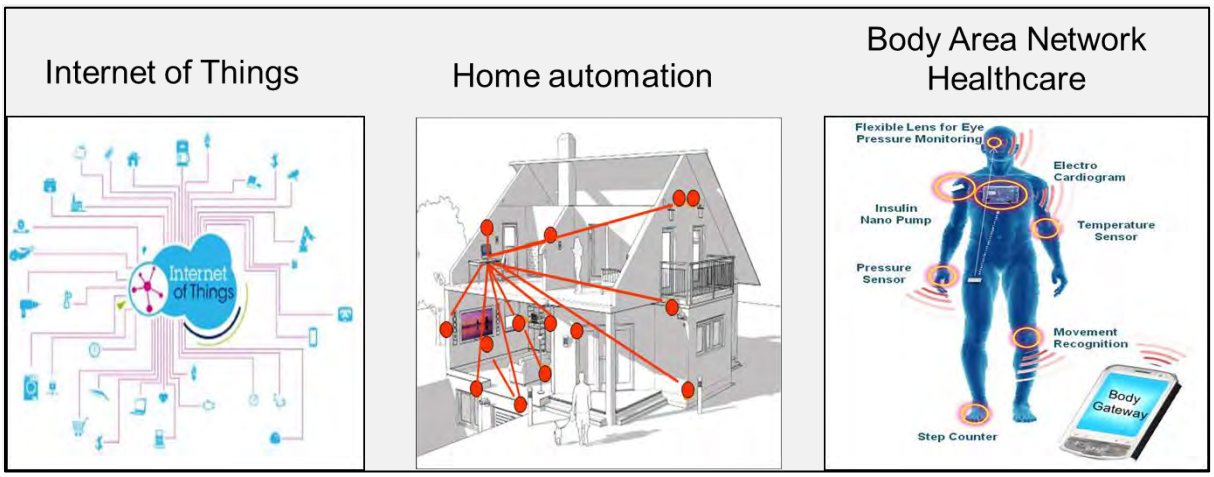


But a smart sensor is not an isolated element. It is an element of a system that constitute an application. The system may be quite simple for the measurement of the heart rate of a runner or quite complex as illustrated in next figure (e.g. for the global monitoring of the physical condition of a team during a football match)



2.3.1 Applications needs

The expected economical and societal impacts of smart sensors[1] applications are huge. The yearly market growth rate for smart sensor related semiconductors is expected to lie between 10% and 40% depending of the application domain. Miniaturized healthcare monitoring sensors will contribute to maintain patients out of the hospital and reducing the impact of healthcare on the national budget. Autonomous sensors will avoid heavy cabling in cars and thus reduce their weight and fuel consumption. Applied to buildings, smart sensors are enablers for intelligent lighting and temperature control. Other applications are the monitoring of the structural health of bridges or windmill motors, the control of the irrigation or watering of soils in agriculture, the lighting-on-need of parking and public places for minimizing the power consumption and for improving the security, etc…



A smart sensor will rely on various heterogeneous technologies like analogue, digital and RF (Radio Frequency) electronics, such as MEMS (Micro Electro Mechanical System)

[1] A smart sensor is made of a measurement chain composed of a sensor (also called transducer that transforms the sensed parameter into an electrical signal), some analogue conditioning electronics, a processor and a wireless transceiver as well as a power distribution chain composed of a battery or energy scavenger and of a power management unit.

or photonics for energy scavenging and chemical for the battery/power supply. It may also rely on fluidics, pneumatics, optics, chemical, biochemical or mechanics for the transport of the samples to analyze and for their characterization. The link of the smart sensors with the domains of heterogeneous integration and smart energy is obvious but some other more specific research domains should also be considered. These are: energy scavengers, transducer and actuator technologies, low-power communication protocols for low duty-cycle smart sensors, low-leakage components, low-power sensor node architecture, modeling and simulation technologies…

2.3.2 Current position

"Smart sensors" is a rather new application domain. Current applications are limited to some specific cases: with high added value markets like the industrial market (automation…) and health market (hearing aids). Current products are rather expensive, generally power hungry, and exhibit large size…
The number of potential applications is rather large but entering these markets could mean cheaper, smaller size, lower power, integration of new technologies…
In order to enable the realization of these new products, effort is needed in various technological domains and this effort cannot be supported by a single partner… Therefore cooperation will be instrumental in making progress in this domain for European industry

2.3.3 Future vision

This multiple integration of a variety of technological options and the request of autonomous energy efficient smart systems requires strong academic industrial collaboration research. In particular, the **long-term R&D efforts might include 3D smart multi-functional materials and novel circuit architectures, sensors & actuators integrating multi- functionalities** (mechanical, biotechnology, nanotechnology, photonics….) **and ultra-low power solutions.** Modeling, simulation and characterization of such a kind of integrated multi sensor have to be performed and experimental progresses have to be evaluated in an industrial environment. MEMS based smart sensors technology opens the door to a new generation of micro-nano scale, innovative sensors to serve key market applications in Automotive, Industrial, Consumer, Telecommunication and Medical markets.

2.3.4 Areas of Cooperation

The need for integration of various technologies and the request for autonomous energy efficient smart systems require strong academic industrial collaboration research. In particular, the long-term R&D efforts might include:

- **Nanoscale structures:**
  -Nanowire, carbon nanotubes, graphene for improving intrinsic device performance or for enabling new functionalities
- **Ultra low power solutions:**
  - For electronics, for software and for wireless communications
- **Integration on/within textile**
- **Implantable sensors:**
  -Biocompatibility and interfacing electronics

-Modeling, simulation and characterization of integrated multi sensors for experimentation of for evaluation in an industrial environment.

- **Heterogeneous smart sensors:**

-MEMS, biotechnology, fluidics…) for applications in automotive, industrial, consumer, telecommunication and medical market

- **High efficiency,** low-leakage (thin, flexible, printed) **batteries**
- **Standardization:**

-Communication, hardware and software interface between key building-blocks

- **Micro storage devices, architecture and materials**

2.3.5 Towards Roadmaps-Proposed methodology

The application space of "smart sensors" is very broad and each application has its own specific requirements. Although the global architecture is similar for all applications, there is no single design that can satisfy all applications. A "smart sensor" application could rely on various technologies, but all of them are not necessarily needed for each application. What is more when a set of applications requires the same technology, all of them do not necessarily require the same maturity level or the same performance level for the needed technology.

As a consequence, the roadmap for a given application (or set of applications) cannot be dissociated from the roadmap of its enabling technologies. The application roadmap of some promising applications should be consequently linked with the roadmaps of the "smart sensor" enabling technologies. Taking into account the number of scenario related to the applications requirements and their associated targets, we have agreed to limit our work to the definition of the methodology to be used. Detailed road mapping activities have to be pursued in the context of ECSEL, CATRENE and HORIZON 2020.

Proposed methodology: we have to combine following three different point-of-views and to combine them into a single view for each considered application.

- **Applications point-of-view**

Looking at the most promising applications (market potential, added-value for the consumer, sustainability, for taking a world leading position…)
Looking long-term with intermediate steps…
➔ Result: list of promising applications

- *"Architecture and building blocks" point-of-view*

Looking at the smart sensor architecture and its critical building blocks
→ enabling new applications (although the ones we are not able to think about, today)
→Result: list of new enabling building blocks

- *"Enabling technologies" point-of-view*

Looking at the technologies (not necessarily specific, incl. tools, standards) that will enable the realization of smart sensor applications
➔ Result: list of enabling technologies

Point of-view Applications

The Preliminary list of sensor networks application is based on the ontology from Libellium (http://www.libelium.com/top_50_iot_sensor_applications_ranking/) and Beecham Research (http://beechamresearch.com/article.aspx?id=4)

- Medicine & Health
- Automotive & Transport
- Plant construction & engineering
- Materials testing
- Process and environmental monitoring

The domains of applications and the related products are very broad with large diversity in their requirements; moreover the technological improvement (roadmaps) will not impact the progress in all application domains in the same way.

Some of the product requirements are depending on the progress made in the technological domains (building-blocks and technologies). The technological progress in the various technological domains will be evaluated in term of the main sensor application drivers, which are:

-Physical properties (size, form factor, readiness/flexibility/stretchability for integration in textile…)
-Power consumption (mean, peak, towards autonomy by harvesting)
-Cost (initial cost, incremental cost…)
-Functionalities (sensed parameters, precision…)
-Infrastructure deployment readiness (servers, communication, IoT, supportive tools & modeling…).

Point-of-view Architecture

Considering that a conceptual architecture is common to all applications, it will be relevant to develop a common platform that will be modular. The main merit of this approach is that whenever a block has been created it can be used in another application.
For this purpose it is needed to:

-Define standard interfaces (mechanical, electrical, software)
-Develop simulation tools

New building-block or adapted building block will be developed for improving specific performances in particular the autonomy (harvester), the power consumption (…), and the functionalities (transducers).
These are:

-Energy harvesters
-Energy conversion ((AC/DC, DC/DC) & management (consume nothing when doing nothing)
-Energy store (low-leakage high-capacity super-capacitors, batteries…)
-Transducers (CMOS sensors, gas, ultra-sound, accelerometers…)
-Actuators
-ULP transducer interface electronics and A/D converters

-ULP processors/controllers and memories (Non-volatile)
-Wireless transceivers & communication stack

Point-of-view Technologies

Necessary technologies are related to:

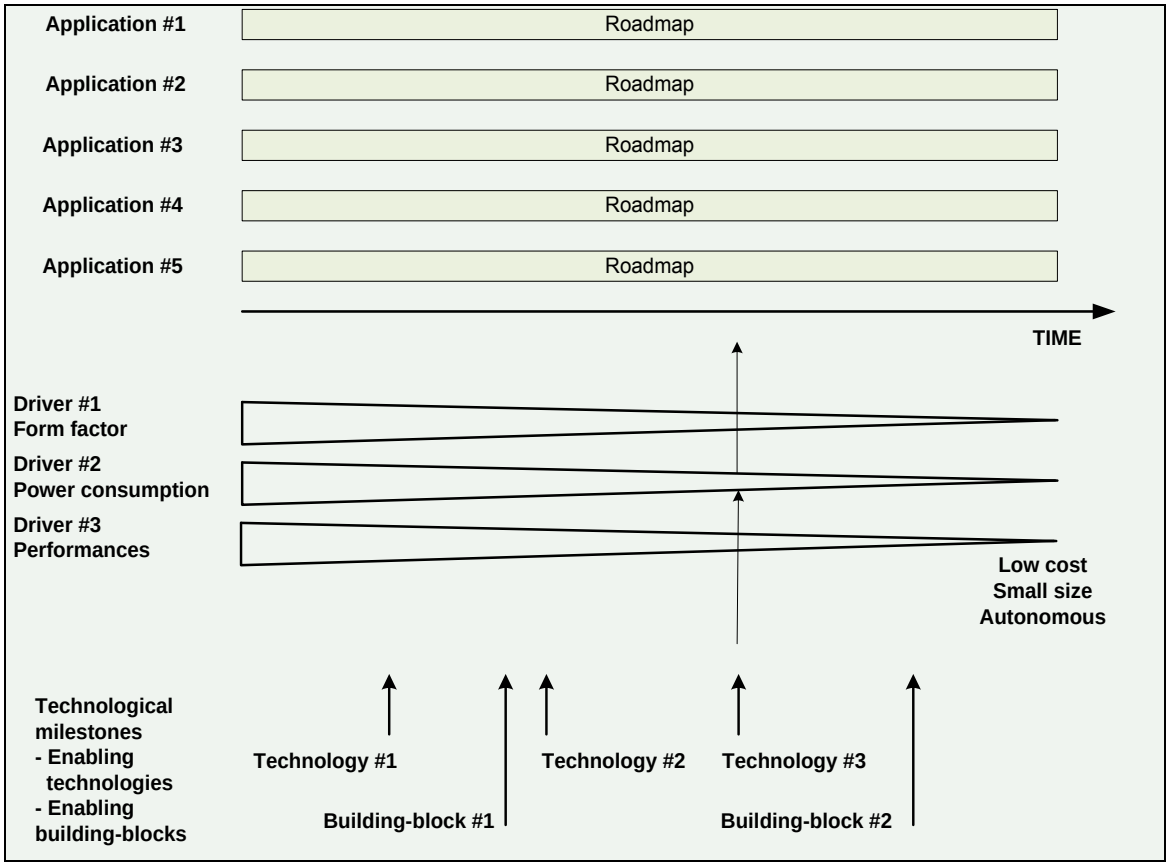
- MEMS
- Reconfigurabilty
- Ultra low power electronics
- Ultra-low power communications
- Miniaturization & integration
- Integration within textiles
- Power management
- Processes & Tools
- Modularity & interface standardization
- Nanoscale structure

--Software technologies (Security, Service deployment, Data mining, database, IoT, User interface)

Towards the roadmap

We propose to start from the application point-of-view (top-down) by elaborating applications roadmaps in some selected domains and to go further with architecture and technology points-of-view (bottom-up) in order to elaborate technology roadmaps.

We will combine top-down and bottom-up approaches with relations to the critical systems requirements specific to each category of application and dependent of the necessary technologies. This approach will allow the selection of the appropriate technologies in terms of cost, schedule and performance.
Following figure illustrates the proposed approach:



3. Heterogeneous Integration

3.1 Applications needs

Depending of the application it is used for, 3D integration could present for an application one or more advantages:
-Improved form factor (3D instead of 2D, smaller volume)
-Improved performance of interconnects (shorter than wire-bonding for TSV)
-Ease of heterogeneous integration (Analog, digital, mechanical…)
-Modularity

The full potential of 3D heterogeneous integration can only be demonstrated for the applications that can valorize at least one of its advantages. Additionally, if the application is demonstrated to work in the same way as its two dimensional equivalent, it will then present a competitive advantage over its 2D-equivalent. It is therefore important to select the potential applications on the basis of the added-value 3D-integration can bring to them.

The ENI2 core group proposes to **focus on three categories of applications**, each of them built on a specific advantage of 3D integration, in order to demonstrate the applicability of 3D heterogeneous integration to the requirements of these application domains. These are:

- For improving performance of interconnect: Computing (mini-server, APs, HPC)

- For improving the form factor (smaller volume): Interfaces (Haptic, Sensors, Hearing aids)
- For demonstrating heterogeneous integration and modularity: Smart energy

Each of these applications will provide different design and realization challenges depending on their functional and nonfunctional requirements related to their different functional blocks (digital/RF, digital/memory, digital/photonics, power management, etc…). These challenges concern among others power, electrical parameters, form factor, cost efficiency, and thermal management.
The search for a solution to these challenges will create opportunities to evaluate the relative merits of each of the technologies supporting the various 3D heterogeneous integration strategies like interconnect, underfill, RDL and many more as well as to identify the potential gaps between requirements and technological potential.

The objectives of the collaborations will be to demonstrate at silicon level the added value of 3D heterogeneous integration compared to the state of the art. The design of this demonstration should be supported by a generic design platform (methodology and tools).

3.2 Current position

Moore's Law describes a long-term trend in which the number of transistors on an integrated circuit has doubled approximately every two years to generate **smaller**, more **powerful** and **less expensive** product. But at the moment the implementation of **Moore's Law** is reaching its limits on various points-of-views. These are:
-Its **physical limits** in relation to the substrate: at 20 nm, the CMOS channel length is about 40 times the interatomic distance of the silicon crystal. Reducing further the size of the channel has thus a negative impact on the **leakage** of the chips.
-Its **physical limits** in relation to the manufacturing process: The importance of the diffraction caused by the edges of the mask is proportional to the wavelength of the illumination light. This is the reason of the progressive shift from visible light to extreme UV illumination for lithography while the size is shrinking. Reducing the size has thus a negative impact on the **cost of the tools** and on the **process complexity**.
-Its **economical limits**: Going to smaller size requires not only a shift to shorter wavelength lithography but also to an improved precision of alignment tools which impacts also the **cost of the tools** and the **cost of the masks**. This has also a negative impact on the cost of the fabs which requires **huger capital investments**.

The nanotechnology industry is looking for a **complementary approach** to the traditional two-dimensional 2D concept that will enable the continuation of Moore's law in the third dimension (3D) through the manufacturing of devices with a still increasing number of elements per unit of volume.
This complementary 3D approach should allow:

-The improvement of the performance of the chips at the system level (enlarged bandwidth, enhanced speed, reduced power consumption)
-The integration and the reuse of existing IP from different technology platforms e.g. heterogeneous digital ICs like 130nm and 45 nm, MEMS, analog IC's, optical, etc..
-The reduction of the form factor through shrinking feature sizes and through appropriate product partitioning

-A cost structure in line with the added value of the final product (some reduction could be due to some enhancements such as the reduced number of metal layer, the increased yield or the faster time to market)

Nevertheless, **3D** heterogeneous integration still **faces a lot of challenges** and the deployment in **volume manufacturing is not** currently **a reality**, despite several large collaborative projects taking place on the subject. Many different technological options have been proposed to support a large variety of applications. Nevertheless, the added value of 3D heterogeneous integration in terms of system cost and system performance has not yet been demonstrated. Beyond partitioning, testing and thermal challenges, three-dimensional integration at the system level is also suffering a lack of common standards, qualified products chains and 3D specific tools at both hardware and software levels.

3.3 Future vision

Due to a lack of cooperation, the European industry has not been able until now to reach the critical mass and the long term vision needed to build an obvious leadership in 3D heterogeneous integration at the research level and to drive this leadership into a recognized manufacturing environment.
The worldwide competition is announced and the need to cooperate within Europe is more urgent than ever in order to avoid to be excluded from the game.
T**he objective of the core group is to define a methodology that will demonstrate the potential of this technology and that will facilitate and accelerate the take up of this technology by the IC companies.**

The core group agreed on the following approach:

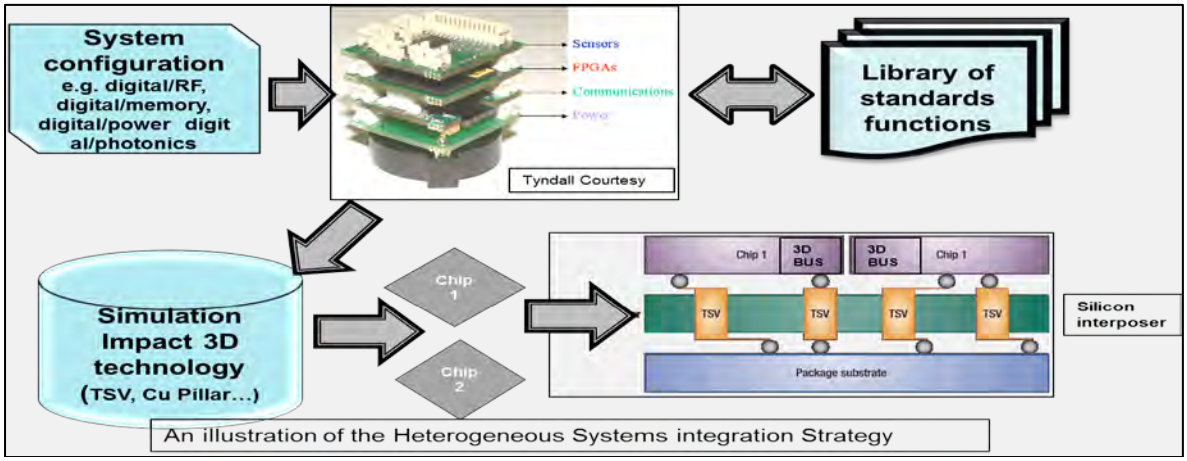
-The technological developments have **to be driven by applications**
-The applications have to be selected according to the added-value 3D integration brings to these applications
-The link between applications and technologies must be clearly stated
-The demonstration of the added value (including cost analysis) must be done at system level and by selecting the relevant building blocks
-Technological roadmaps will be created and gaps/roadblocks will be identified
-Building block implementations will be supported by generic design platforms

3.4 Areas for cooperation

- **System level prototyping tool: European library of re-usable functions**

The heterogeneous integration potential can only be demonstrated if the correct applications are chosen and can be demonstrated to work in the same way as their two dimensional equivalent. It is therefore important to choose a number of potential applications and evaluate them for their suitability for integration in 3D. There are some applications which will be suitable for this and others which will not. However, until the design process is started it is hard to know which ones these are. **We need to address the issue by developing a low overhead prototyping tool which may provide some insight into the potential for integration** and allow evaluation of a system in its

application space without needing to go through the technological challenge of building it in a 3D integrated process. For a specific required function or component specific application, it can be designed to comply with the interconnection protocol and used interchangeably in the system in conjunction with all of the other system blocks. The main merit of this approach is that whenever a block has been created it can be used in another application. **This therefore should permit the creation of a European library of functions.** This approach will help the design and the modeling of 3D heterogeneous integration product in different ways:



-Different system configurations can be studied and digital/memory, digital/digital functions…can be addressed. This will help to define the best architecture
-Check mission profile: design simulation will be faster and reliable due to experimental fits
-Detect challenges in power management: hot points can be identified and dissipated by design
- Reliability can be anticipated: both electrical and thermal wearout can be checked through operating life test.

- **3D design**

In addition to the urgent problems from the actual implementation of such systems (place & route, testing, design kit..) we see an additional need for **EDA methodologies for bringing the system description towards an accurate implementation.** Aspects to be regarded at the system specification include separation of functionality to the dies, rough floor-planning of the dies while regarding communication function (on die and via TSV), allocation regarding thermal constraints and testability of the later devicesto enable the design of complex 3D integrated systems, the specific requirements and boundary conditions coming from 3D integration have to be considered in all stages of the design process.

- **3D Integration**

TSV technology

Cooperation must be reinforced in TSV and 3D interconnect technology to improve the TSV formation processes flow challenges (need for a more standard process), as well as making them more economical and new solutions need to be found which can reduce

the stress induced by the TSV. At the interconnect level new research has to be conducted at bonding and electrical interconnect level. Furthermore all aspects need to be considered from a reliability perspective.

Interface standardization
In current CMOS technology the interface of the IC is located at the level of the package description as the realization of an IC is generally done and owned by a single IC manufacturer. Moving to more-than-Moore and realizing a 3D-stack integrating multiple heterogeneous dies (MEMS, Analog, digital, optical…) requires a multi-disciplinary expertise that is generally not held by each of the individual manufacturers. As a 3D-stack is expected to include the components from different manufacturers **the interface should be defined at the chip level for mechanical, electrical and software aspects.**
The standardization of the 3D-interface presents also some additional advantages like die-reuse between products, ease of upgrade to a new product generation, independent design of each of the stack elements, faster time-to-market…
Standardization of the mechanical interface is of course also needed for the realization of the production tools.

Thermal design tools
More-than-Moore means a 3-D package with a progressively increasing number of transistors per unit-of-volume and consequently an increasing heat generation per unit-of-volume. A **specific attention is therefore needed to low-power-design,** to the right distribution of heat generation (avoiding hot spots) and to a careful design of the heat evacuation system when needed. The thermal design should be supported by appropriate design tools.

Novel material for 3D Integration
Several of the hurdles that have slowed down the adoption of 3D technologies are material related: existing materials for temporary wafer bonding are immature and lead to yield loss, under fills, Thermal Interface Materials and Molding compound are insufficiently capable to conduct heat away from the IC during operation, under fill materials need to evolve in order to enable wafer-level or gang processing in order to contain cost of ownership of 3D-integrated devices. Therefore ample opportunities exist for development of new materials that enhance reliability and cost of ownership of 3D systems.

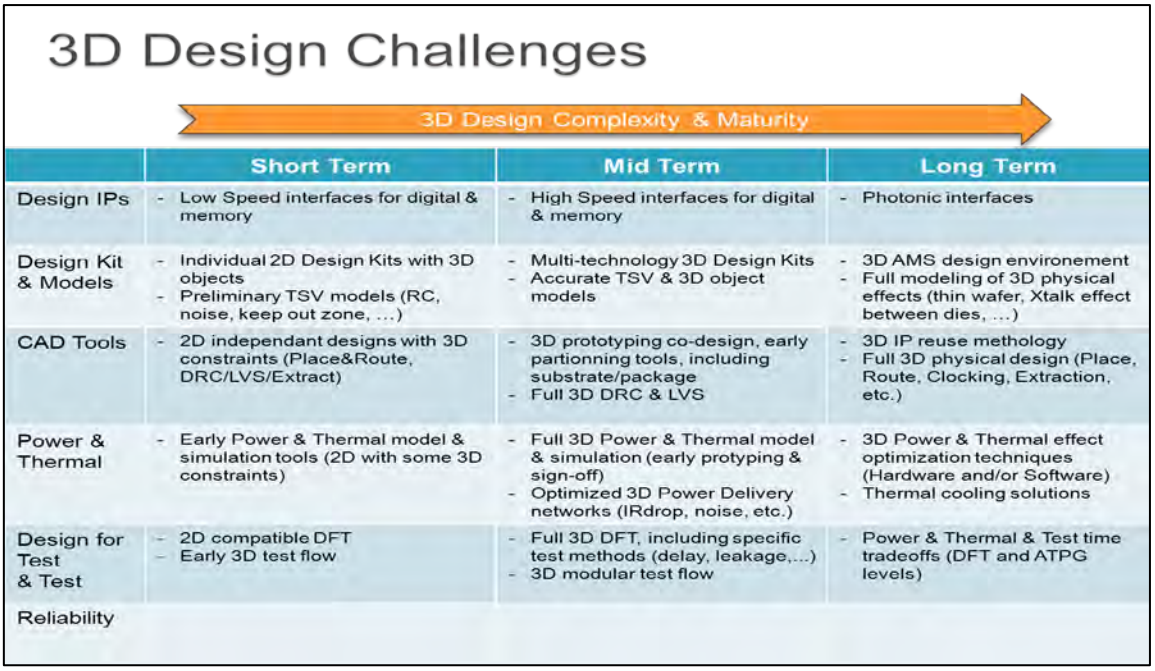
3.5 Roadmaps

As an intermediate step towards full scale 3DIC integration, the core group has agreed to base the European collaborative roadmap on existing IDM infrastructure as far supply chain and process **(Assembly, test and reliability)** are concerned.
The objective is to match the product vision of systems companies, which are continuously required to add new functionalities, reduce cost and time to market, to the economics of implementation methods.
To do that, **the 1st R&D&I topic** will be to make up, at European level, **a library of functional** blocks and to define and associate **standardized interfaces**.
The 2nd element will be based on interposers (silicon, glass, organic...) with TSV included

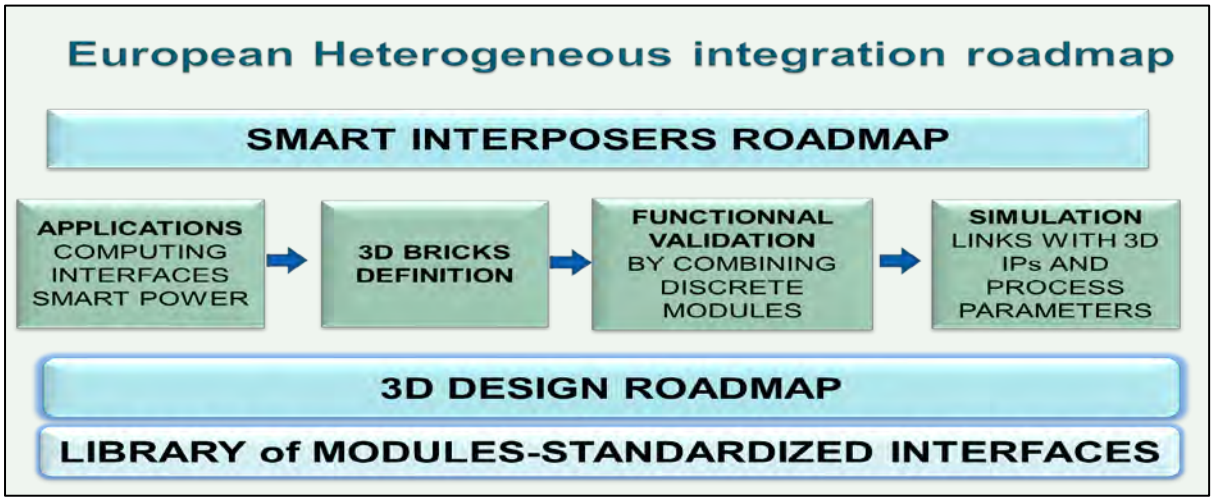
The 3rd element will cope with the design platform methodology and tools that allow a seamless heterogeneous system design.
The last element will address the technological gaps.

The Figure below illustrates the approach to be taken in this domain and shows the four different levels of development required to achieve a complete strategy for heterogeneous systems level integration.

SYSTEM LEVEL INTEGRATION	-Applications need analysis. Extraction of relevant parameters	- Library of functional validation blocks -Behavorial models	-Modeling of the influence of integration on the system behavior
SMART INTERPOSERS	RDL Interposer - Multidies, TSV, Double side	Passives Interposers -Passive in RDL-Mems clocks-3D capacitors-Antennas Thermal interposers - Passive thermal enhancer -Active cooling	Active interposers -Power management -High voltage -external I/O Photonic Interposer - Photonic converter -Chip to chip link -Alternative material to silicon
DESIGN	Detailed roadmap below		
3D INTEGRATION **TSV & Interconnect**	-Cost efficient of TSV formation process steps -Chip packages integration issues	-Alternative TSV etch and filling process -Thermo fluidic mechanical design and modeling -Influence of TSV on processed chip performance - Impact of bumping/ interconnect processes on devices - Stacking processes: underfill materials, strategy for multidie stacking, Die to Die or Die to Wafer stacking	-Materials for reliability /lifetime -Impact of TSV on self-heating in SOI circuits - “low T, low P, 10ms bond process



The proposed global approach shows the different aspects of the heterogeneous systems integration challenges that need to be addressed in parallel to create an industry in Europe that produces and sells miniaturized systems based on the heterogeneous integration of mixed technology devices.



4. System integration

Development complexity and scope of embedded systems design are increasing at a staggering pace due to the combination of hardware and software components, the continuing increase of number components on a chip and the integration of analogue functionalities.

Europe needs to drive the development of the technologies that enables its semiconductor companies jointly with system solution providers and academic research centers to overcome the design challenges and to create innovative and cost

effective solutions for tomorrow's silicon based systems. It calls for the widespread development of standards and interoperable techniques at the device and application level. These would allow dynamic markets for integrating new kind of products from state-of-the-art components with fast time- to-market.

European companies show that they are ready for this cooperation. Such standards and techniques can later appeal to other geographical markets (US, Asia) while giving an edge to Europe industry; standards and interoperability also strongly facilitate the entry and thus the emergence of SMEs.

The objective of the System integration is to identify the long-term areas of cooperation enabling a better alignment and the cooperation between Applications systems companies and IC providers.

4.1 Applications needs

Systems are continuously getting more and more complex and the integration level of system blocks is higher. Furthermore, the requirement set is increasing, or requirements might be even unknown at the design phase: end-users may download software that is not foreseen in requirement specification.

The different design cultures (languages, internal processes, design practices, documentation, etc.) of the players introduce, however, easily challenges related to compatibility of the design modules and processes. Consequently, integration and verification time and effort are exploding, while integrating external IP stays a risky undertaking.

Future highly featured electronic products not only will comprise very sophisticated and extremely complex embedded silicon systems but will also integrate solutions from different technological domains. This shall allow extremely compact systems combining extraordinary multifunctional services with very convincing form factors, e.g. a very handsome all-in-one mobile service device for, cellular phone entertainment, access

control, payment, medical assistance, orientation in cities etc., but also safe and efficient mobility devices (cars, motorcycles, etc.) with all relevant functions in very few control units, little mechanics and mostly electro-mechanical actuators. In addition, the mobility challenge focuses on balancing hardware and software integration, removing overhead from today's strongly heterogeneous systems, thereby growing efficiency, and safety on the move.

From system architecture and integration perspective the key issues are:

- An executable and unambiguous Electronic design model representing the functional and non-functional needs.
-Automatic and semi-automatic verification/validation methods are required to reach higher of confidence in Systems behaviors especially trust and control in highly critical scenario (automotive, avionics…). Moreover, verification and validation are not aligned.
-Performance modeling covering both functional and non-functional properties are time consuming and inaccurate.
- Design productivity (digital & analog) and cost effectiveness is suffering of a lack of standards

4.2. Current position

Today various platforms have been developed in order to speed up system design and simulation. Some of them are now very popular but none of them have been able to establish as an undisputed solution for the development of new system on chip. There are several issues which needs to be addressed simultaneously by the solution making the range of problem to be cover extremely large and very often incompatible one to the other. Below are described the most important ones.

- *Increase in complexity*

Today modern systems cover a lot of different domains from RF, mixed signal solution for energy management, mechanical with integration of new sensors, and digital for very powerful processing. The design of a new system needs to make a tradeoff at architectural level between a large numbers of parameters. It is only if all of these parameters, or at least the most important ones, are taken into account that it is possible to specify a system with good performance in an acceptable thermal and power budget. Unfortunately it is today very difficult to find a platform able to cover all these domains making system trade-off extremely challenging.

-Large number of parameters

The variety of domains to be covered simultaneously has drastically increased the number of parameters to control in order to properly size a system. All of these parameters have different representation with very different levels of abstraction regarding their behavior. The modeling of a large system needs to connect together all of these parameters to give a synthetic view to the architect/designer in order to make the right decisions. The increase in parameters has drastically increased the architectural space making its investigation very difficult. It is then very important to have methods allowing fast simulation in order to reduce as much as possible simulation time making possible a large exploration of the architectural space. It is not today always the case and very often a very limited part of the complete space is explored which could lead from time to time to low performing solution.

-Software driven systems

Today systems are embedding more and more processors. This has an effect of making software a very important if not the most important part of the system.

-Abstraction level

Due to the large number of domains which need to cooperate together, it is extremely difficult to have the same level of abstraction between all of them. Making really system design needs today the assembling a heterogeneous tools. In these conditions it is very difficult to have a seamless connection between them making sometime the work of architects/designers very painful. System C-based methodology was proposed some years ago as a possible way in handling the system complexity. Using System C is possible to build virtual platforms that move earlier in the design flow the activities related to architecture exploration and validation, as well as embedded software development. System C through the standardization of several TLM type of modeling is able to effectively model hardware components at different abstraction levels for memory mapped bus systems, **but System C** is still suffering of a lack of standards for other types of communication, which **limits model-to-model interoperability**. This impacts the efficiency of system integrators, as seamless integration of third party models into virtual platforms is yet to achieve.

Another limitation to the growth of the virtual platforms ecosystem **is the lack of standards** addressing the interactions between models and tools. So far, a tight dependence link exists between CAD tools and proprietary modeling objects that negatively impacts model-to-tool interoperability, and consequently prevents a wide deployment of these platforms. Extending the standards in this area will be beneficial to platform integrators and users, by providing a wider offer in term of tools, as well as to EDA vendors, by extending the market opportunities for their analysis tools.

The ever increasing number of IPs and subsystems integrated in SoC directly impacts the intrinsic complexity of virtual platforms and consequently dramatically reduces the overall simulation speed. **In the future, efficient simulation frameworks should support the distributed execution of complex virtual platforms** which will require addressing technical difficulties related to the model of computation currently adopted for these platforms.

System Verilog is gaining ground in the system verification area to define complex test benches, considering the adoption of the UVM verification methodology. However, a large variety of languages are used today to build verification environments (C/C++/SystemC, HDLs, Perl, python, etc.) and they hardly interoperate. In order to maximize verification IP reuse and increase efficiency of verification engineers, **multi-language standard-based verification environments are still to be invented.**

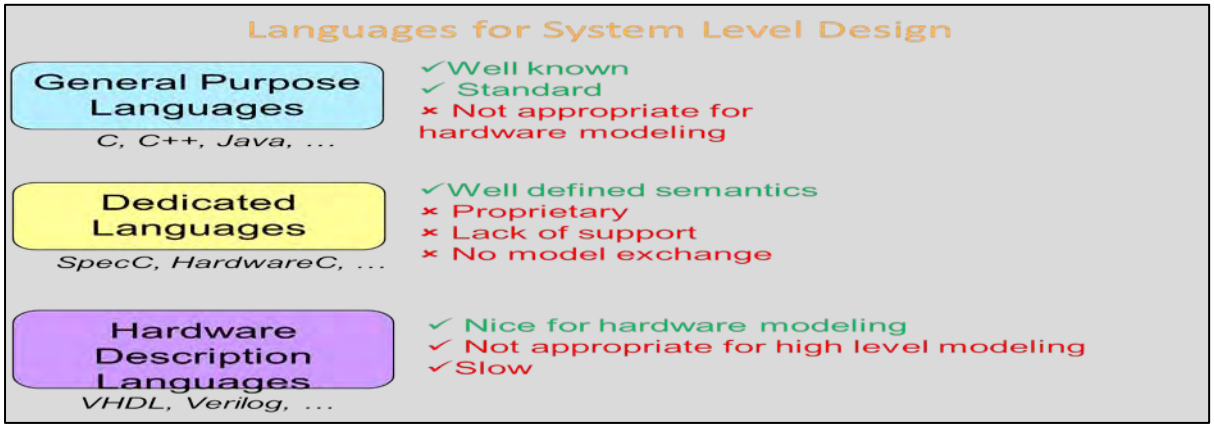
TLM is used as a method to increase the level of abstraction of design entry to cope with the complexity of systems. This has been a major breakthrough, shifting the level of abstraction from the RTL level up to the architecture level. **This is now required to shift** again to the next level, **addressing** in a holistic way **system specification and verification**, expression of system use cases and constraints on design resources to address the environmental requirements for low power devices. These sign-off executable models between system houses and semiconductor companies shall be the design entry point to generate the various design views (virtual platforms, software, hardware implementation) and keep them consistent throughout the design process.

The Spirit consortium and afterwards **Accellera** have developed the **IP-XACT specification** that describes a standard way documenting IP meta-data for Systems integration. This is a key element to automate IP integration, and can be seen as a pivot representation at the architecture level to support generative flows. However, **lacks in the standard** (e.g. easy support of generic IPs, no support of extra-functional attributes in the meta data) **are limiting** the adoption and **the deployment of these descriptions by IP providers**, which impacts all the value chain. Connections with other standards like UPF should also be considered to address the requirements of low power devices.

Despite an intensive industry activity, **standardization is still in infancy** and there is still a lot to do to develop a European framework overcoming the difficulties faced by the Systems designers in integrating IPs coming from different sources and developed with different design methodologies and software architecture.

4.3 Future vision

A new design flow generation, including new design tools, is required to facilitate the platform development **starting at higher abstraction (system) level instead of IP level**. New frontier can be defined that extends standard lightweight software modeling methodologies like UML to apply them as higher languages operating in synergy with the lower level languages. Thus SoC new flow should be able to exploit formalism and conventions that may be found in UML, mathematical models, Esterel, SDF, metamodel etc. as an entry point. Furthermore, these models should be transformed down to the well accepted descriptions like SystemC/TLM, XML-based IP-Xact or a possible new evolution.



In order to increase design productivity, some specific functions can be synthesized in hardware blocks thanks to the use of high level synthesis tools. The same approach can be followed for the SW and use tools for code generation. Both approaches provide a way to cope with complexity and handle derivative platforms.

New verifications approaches should be also introduced, it is not more acceptable (for time to market, quality and costs reasons) to continue to verify the systems at RTL level. This implies the need **to move from current description languages** used at RTL (VHDL, Verilog, System-Verilog) **to higher abstraction levels, at system and architectural level**, to improve verification quality and reducing verification computing time for both HW and SW.

In addition, it will be necessary to develop novel approaches for physical prototyping which are used to complement the well-known virtual prototyping approach. Such novel approaches have to address the functional software validation and early real-time software optimizations.

Finally, but certainly not the last, tools are required for power analysis and verification including system architecture, hardware/software implementation levels, especially critical for the multimedia and telecom mobile platforms.

It is clear that a large number of tools are needed to work together to have a chance to provide an acceptable solution for system level design. As a first step, interaction between the different tools is mandatory and smooth exchange of information between them is a mandatory requirement. Unfortunately, it is by far not enough to provide system designers with a usable environment to develop the very complex system that modern applications are now requiring.

There are 3 key challenges which have to be taken into account and needs a lot of engineering to be addressed properly.

-From top to bottom

From high level to low level models and consistency across the different layers.

-From bottom to top

From low level debug to high level view

-Integration of legacy

In most of the cases, we never restart from the blank sheet (amount of existing IP's, validation, certification…) and we need new methods to integrate legacy and to manage it.

In the todays solution these 3 challenges are partially addressed making deployment of solution sometime difficult when not impossible.

4.4 Areas of cooperation

There are only a few players who can manage entire system design effort alone. These facts guide the players to find appropriate partners to solve existing design or productivity bottlenecks. The different design cultures (languages, internal processes, design practices, documentation, etc.) of the players introduce, however, easily challenges related to compatibility of the design modules and processes. Consequently, integration and verification take more and more time.

In order to overcome the challenges and maintain competitiveness in global markets, a long-term focused collaboration is needed to increase model and tool interoperability for electronic system design at the transaction-level.

Semiconductors Suppliers, EDA vendors, IP vendors and systems solutions providers must come together to share the costs and risks and provide the basis for an eco-system favoring effective collaboration and driving innovation and productivity

We propose to focus the cooperation on three areas:

- **Executable representation of System**

-Model-based design methodology providing an executable specification for the development of heterogeneous functionalities serving as a reference for subsequent design steps.
- Advanced languages to describe heterogeneous Multi-Soc systems at different levels of abstractions
- Automatic generation of virtual prototype directly from high –level Multi-Soc language enabling the analysis of the systems representation as well as its behavior.

- **Evaluation of the System performance**

-To develop verification and coverage techniques addressing both functional and non-functional verifications
-To develop virtual prototyping enabling architectural exploration and results evaluation for hardware and Software linked to architecture specification and system validation
-Ultra-low power hardware design and efficient software for low-power system

- **Design productivity**

-To develop requirements for new/update digital and analog standards enabling European companies to maximize the efficient reuse of internal and external IPs.
-To define and built-up a virtual design platform enabling IP development, packaging, parameterization and integration that are supported by interoperable tools
-To define/develop/deploy and integrated design management system for productivity improvement.

5. Manufacturing science

The semiconductors industry is operating in an increasingly dynamic and unpredictable market context, characterized by very short product development and life cycles and extreme price pressure. Furthermore, the nature of semiconductor manufacturing process introduces a number of challenging issues, which arise from the need to master the complexity of continuous and irreversible multiple processing steps. Regardless of the technologies implemented (logic, memories, analog, bipolar) semiconductor manufacturers are facing a common requirement for increased productivity based on reduced costs, shorter cycle time while keeping environment awareness. The

continuous research of innovative solutions is therefore mandatory in this environment of fast changing paradigms: technology ruptures, new materials, increasing level of automation, myriads of regulations and mandatory code compliances, increasing energy costs, adhesion to the principles for a sustainable development and so on.
Smaller, smarter, faster, cheaper and safer are all serious challenges threatening the competitiveness of the European Manufacturing base and requesting a long-term continuous effort and focused approach in the field of **Manufacturing Science, which is the key strategic differentiator for improving the productivity and thus to be in the position to produce more chips in Europe.** The SMEs, the Institutes and the Academic Research will make a major contribution in achieving this strategic goal.

5.1 Current position

The scaling down of the MOS transistor has driven the progress in the ICs performance and the cost per function of the devices has dropped accordingly. This trend will continue for pure logic devices, but in parallel, for some complex devices, the decrease of the cost per functions will be achieved by the development of derivative options on top of the core processes and the integration of heterogeneous processes. This will lead to increasingly complex line management driven by many process generations, multiple products with short life cycle and high variability in terms of demand. Conventional semiconductor fabrication line management relies mainly on ruled-based heuristics and simulation, and are not enough effective so far: studies show that a wafer spends over 70% of its life time in the fabrication line queuing. This is due to the extreme complexity of the scheduling problem posed by semiconductor fabrication: reentrant flows, multi-purpose equipment, parallel processing within equipment, lack of reliability of the equipment and length of the process flows. The other issue is related to the equipment usage. Benchmark surveys with competitors and foundries in the Pacific Rim show that the overall efficiency of similar process equipment can reach 95% while best performances in Europe are targeting 85% with some specific tools with very high cost of ownership being much below this value.

5.2 Future vision

For effectively managing this highly complex mix of technologies, processes and products, and in order to stay competitive, we need for the manufacturing operations, to develop new tools and methods for fab productivity. Solutions have to be deployed with a focus on eradicating waste in the fab by managing cycle time and advancing equipment and process control.
In particular, controlling process equipment is a massive challenge for the semiconductor industry that can't be solved by IC manufactures alone. While some metrology will always be needed, alternative solutions have to be developed to enable the industry to keep moving forward in terms of cost and device performance. The concept of "virtual metrology" has to be extended and we will have to develop the tools and methodologies necessary to implement a powerful predictive equipment control system, integrated with the line decision systems, which is becoming a "must have" to reduce unscheduled equipment downtime, metrology effort and number of scrapped wafers. The semiconductor industry has to experience a real breakthrough from reactive to predictive factory operations and new way of organizing manufacturing systems have to be investigated to meet the above challenges.

Although the European semiconductor facilities can already be considered as having a limited environmental impact, progresses are still to be made to limit the environmental footprint and maintain the compliance with the European regulation (i.e. RoHS and REACH directives) which is continuously challenging the manufacturing fabs to reduce their environmental impact while maintaining their competitiveness with other regions.

5.3 Areas of cooperation

To improve its manufacturing effectiveness and to stay competitive, the semiconductor industry must benefit from a converging network of experience and competency involving the academic community, who is active and competent in the field of applied mathematics, statistics and modeling, the decision and information systems providers capable of developing advance software solutions, and the equipment makers to support the required evolutions of the process equipment. In this perspective, the **SMEs will bring a major contribution** in particular by their predominant role in the equipment semiconductor manufacturing landscape.

We have to focus combined collaborative resources in the following domains:

- **Factory operation:**

Covers the methodologies and procedures that are implemented to control the production in the fab and are including:

-Reduced cycle times requiring the development of new paradigms and a lot of improvement in the line management and decision systems to make them capable of optimizing the complexity of the resources and material management.
-Factory flexibility to develop solutions dealing with the ability of a production system to change the mix, volume and timing of its input.
-Fab simulation model to predict waferfab future performance, e.g. detection of forthcoming bottlenecks in case of systems changes such as different queues disciplines and job priorities.
-Data mining: to develop data models able to encompass work in progress, move, capacity, wafer outputs, cycle time ….and associated variable internal/external factors such as yield, learning effects, market demand….
-Scheduling: to develop scheduling/rescheduling methodologies ensuring that the equipment are available at the appropriate time.

- **Production equipment:**

Efficient control of production equipment is central to improve the reproducibility of the manufacturing process and the equipment effectiveness. Thus two domains of collaboration have to be supported:

-Virtual metrology to develop models predicting the metrology measurements from process parameters and sensor data from the processing equipment.
-Predictive maintenance*:* to develop Predictive Maintenance (PM) techniques to improve the process tools reliability whilst optimizing availability, utilization and overall equipment effectiveness.

- **Material Handling Systems:**

New analytical and simulation models of MHS need to be developed to understand the behavior of such systems and bridge the gap between theoretical research and industry problems.

- **Factory Control system:**

In-situ feedback control new sensors have to be developed. In parallel, sophisticated fault detection isolation accommodation algorithms have to be implemented throughout the fab, and complex closed-loop control systems have to be developed. Progress in equipment scheduling and Advanced Process Control (APC) has to be pursued.

- **Environment, Health & Safety**

Design, development and assessment of innovative and comprehensive approaches to reduce the environmental impact of existing semiconductor fabs with a focus on solutions for the reduction of water and energy consumption,

SUMMARY OF THE KEY AREAS OF COLLABORATION	MM (1)	MtM (2)	Equipment	SMEs	Universities.
FACTORY OPERATIONS					
Flexible Line Managment	+	+		+	+
Scheduling tools	+	+	+	+	+
Single Wafer lot processing	+	+	+	+	
Fab modeling &simulation	+	+		+	+
Data Mining	+	+	+	+	+
PRODUCTION EQUIPMENT					
Virtual metrology	+	+	+	+	+
Predictive maintenance	+	+	+	+	+
In situ sensors & equip data	+	+	+	+	+
MATERIAL HANDLING					
Tool to Tool transportation	+	+	+	+	+
FACTORY CONTROL SYSTEM					
Real time systems to control process variation	+	+	+	+	+
Factory systems to equip./AMHS interfaces	+	+	+	+	
Full fab integration	+	+	+	+	
ENVIRONMENT HEALTH & SAFETY					
Energy saving solutions	+	+	+		
Abatement Systems	+	+	+	+	+

(1) MM: More Moore
(2) MtM: More than Moore

6. Ecosystems-Research Infrastructure

6.1 Definition

Under a very broad definition of infrastructure, there is no MNT infrastructure in Europe.
Infrastructure for industrial R&D is often different from the infrastructure needs of academic research. Infrastructures **can be for science** but are often needed **also for innovation** developed through the **collective production of knowledge**. ENI2 is not focusing on infrastructure in the sense of bricks & mortar or equipment: it is a broader initiative to create a strong and lasting R&D ecosystem and associated competences centres in nanoelectronics involving the 3 pillars of R&D – academia, RTOs and industry and guided **by common objectives to overcome geographical barriers.**

6.2 Structuration

The Roles in a 3 level Infrastructure for innovation have been defined as follows:

1st Level: Academic Labs

- Conducting studies in parallel of basic material properties, deposition and etch techniques etc… or of new device concepts (ex: memristor, MTJ, Power…) or of new electronic functionalities (ex: 3D image coding, neuronal network, power processing architectures and systems…..).

2nd Level: Integration Institutes

- Offering technological capabilities to deliver a complete module (process or device) with characterized performances.

3rd. Level: Industry Relevant Implementation Centers

- Capable to bring the new concepts to the industrial volume level for the functionalities or capable to integrate new modules in full fledge (design rules, models, reliability, manufacturability, process control …).

EXAMPLE OF OPERATION ON HYPOTHETICAL BUT REALISTIC TOPIC.

OBJECTIVE: integration of spintronic on CMOS

Level 1: Labo academic: spin property of thin film magnetic memory concept point using the spin (Magnetic Tunnel Junction)

Level 2: Center Integrator: implementing the technology to small scale of MTJ on R & D equipment demonstrator (standalone) low density, performance, reliability model.

Level 3: industry relevant implementation Centers: Integration in the path of a multilayer CMOS non-volatile magnetic memories; optimized architecture, product design, performance, miniaturization.

Same principle applied to PCRAM, optoelectronics, sensors, MEMS …

The concept of selecting technological options through a filtering process is not new and is informally applied in many places. In France, the project NANO2012 is based on this principle with a limited life span. In USA between SRC/SEMATECH/SUNY-Albany and IBM there is such infrastructure. Many FP, ENIAC, or EUREKA projects, with a well-

defined objective, successfully organize their consortia along the same concept for a limited duration. It was also implemented through the FP6 and EUREKA MEDEA+ projects (Pullnano, Sinano, and Reaching 22) but not organized with long-term objectives.

What is needed is a permanent formally organized infrastructure where long term objectives are shared. The 3 Level Infrastructure for Innovation requires a common vision, a rationalization of effort, a communication process, and sources of funding.

6.3 Ecosystems

The solid collaborative experience acquired through European FP6/CATRENE projects (Nanocmos, Pullnano, Uttermost) in the CMOS domain have strongly contributed to create thrust between the partners and to identify the main expertise by organization involved in the domains/programs/time horizons and in the processing/characterization platforms. The figure below shows the structure of the Nanoscale FET ENI2 ecosystem combining by competences the different research horizon. The ENI2 nanoscale FET ecosystem will contribute to improve the structuration of the Research across the EU. Technology providers will reduce their investments in particular technologies (on the basis that they can reliably access them from an EU partner), permitting all partners to focus and specialize on their core technologies which would complement one another to provide a broad and powerful technology spectrum. In a mid to long term perspective, the result will be several competence centers balancing the scattered aspects of the European Union in combination with a focused approach to be world leader in future high tech markets.

The same approach must be consolidated for the other ENI2 domains.

STRUCTURE OF THE NANOSCALE FET ENI2 ECOSYSTEM COMBINING BY COMPETENCES THE DIFFERENT RESEARCH HORIZON

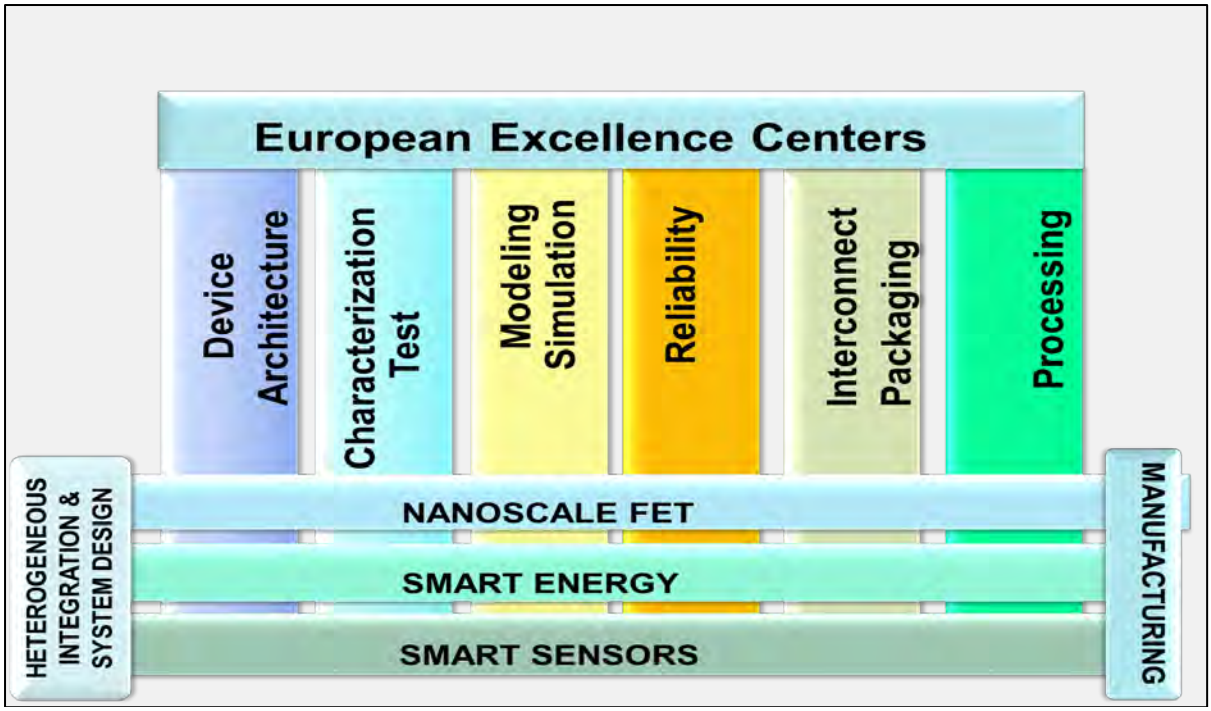
	ULTIMATE CMOS	BEYOND CMOS	NOVEL INTERCONNECTS ARCHITECTURES	ULTIMATE PROCESSES TECHNOLOGIES	3D SEQUENTIAL INTEGRATION
ACADEMICS	Tyndall	Tyndall	TU Delft	VTT	
	FZ Julich	Univ. Stuttggart	Tyndall	Tyndall	
	IuNET	IuNET	Grenoble INP	Grenoble INP	
	Univ.Granada	Univ.Granada	FZ Julich	FZ Julich	
	IMEL	IMEL	Uppsala Univ.	Uppsala Univ.	
	Uppsala Univ.	Uppsala Univ.		KTH	
	Newcastle Univ.	Newcastle Univ.		CNM	
	Univ. Twente	Univ Twente		IMEL	
	URV	URV			
	Grenoble INP	Grenoble INP			
	UCL	UCL			
	ITE	ITE			
	Warwick Univ	KTH			
	Univ. Glasgow	Univ. Glasgow			
	CNM	CNM			
	IEMN	TU Delft			
	IES	VTT			
	Chalmers	ICN			
	VTT				
	TU Delft				
	ICN				
	KTH				
INSTITUTES	FHG	FHG	IMEC	IMEC	Leti
	Leti	Leti	Leti	Leti	
	IMEC	IMEC		FHG	
INDUSTRIALIST	ST	ST	ST	ST	ST
	Thales	Thales	Thales	ASM	
	Micron	Micron			
	Intel	NXP			

6.4 Excellence Centers

Strengthening and focusing Europe's strengths will significantly improve our global competitiveness. "A centre of excellence is a structure where RTD is performed of world standard, in terms of measurable scientific production (including training) and/or technological innovation". **We propose to structure the Competences Centers around** seven main expertises of R&D knowledge: materials, device architectures, characterization/test/assessment, modeling/simulation, reliability, interconnect/packaging, processing, equipment and manufacturing.

The quantification of the RTD degree of excellence should be based on:

-scientific publications ("bibliometry"),
-patents filed,
-number of research personnel and visiting scientists,
-number and volume of commercial contracts,
-number of spin-off companies
-participations in trans-European educational schemes, etc



6.5 Mechanisms of collaboration

As pointed out in this report, the new generations of Nanoelectronic ICs present increasingly multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, etc.) resulting in an urgent need of academic research based on a scientific approach, in order firstly to understand the underlying physical mechanisms and hence to remove the present technological limitation. Industry is indeed, increasingly relying on new ideas and competences coming from the academic community in order to continue technological innovation. This long term research must be supported in order to prepare the path for future information processing technologies, as a 10-to-15 years' timeframe is usually

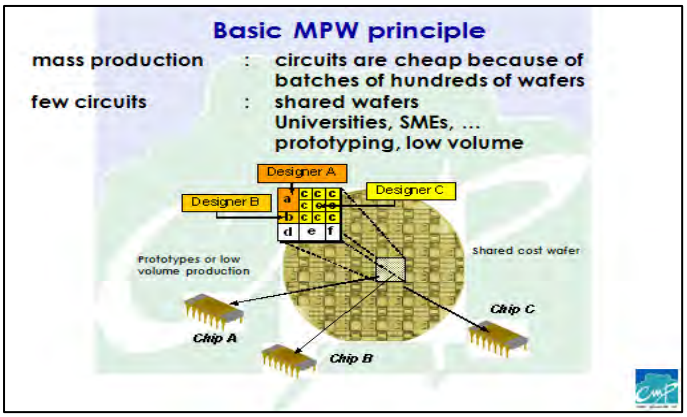
necessary between the first validation of a new innovative idea and its full demonstration and acceptance into complex systems.

In this timeframe, complexity will also derive from heterogeneity, referring to the increasing diversity of functions integrated on to CMOS platforms as envisaged in the "More than Moore" approach. Again, to learn how to intimately combine CMOS with sensors, actuators, MEMS, NEMS and biochips and demonstrate their innovative benefits requires enhancing multi-disciplinary scientific experiments, from design to fabrication and characterization, for and by a large research community.

The realization of these forward-looking activities needs mechanisms of collaboration between the different level of the research infrastructure which will allow rapid prototyping and test of the explosive diversity of materials, technological options and devices, leading to a first validation of the novel concepts. It will encompass state-of-the-art equipment using wafers in the 100mm-200mm-300mm-450mm range.

We propose to base the mechanisms of the collaboration on the FLYING WAFER FP6 project (http://www.flying-wafer.info/), which as a result proposed a model and a concept with the potential of guaranteeing a safe and fast exchange of wafers and data between European R&D nodes to allow multi-site processing. An implementation and a validation phase will be necessary to turn the results of this feasibility study into the ENI2 real cases collaborative environment.

6.6 Routes of access



As part of the ENI2 infrastructure one of the key aspect is the access for European academic institutions and SMEs to the ENI2 technologies. **We need a structure able to offer Multi Project Wafer capabilities** and support a design environment that includes design kit, CAD tools and packaging services. This could be based on the Eurobroker FP7 proposal n°317070 aiming at lowering the access barrier to selected integrated circuits and MEMS processes, by subsidizing the cost of manufacturing **for the benefit of European Universities, Research Laboratories and SMEs.**

7. Impact

The first main direct impact of the proposed infrastructure is to associate in a complementary way interdisciplinary R&D teams to reduce risks, costs and to generate new knowledge to be exploited.

Furthermore by focusing on clear strategic R&D goals, ENI2 will be able to provide **high added value in terms of R&D cooperation results**.

Another key aspect of the expected impact is the potentiality of ENI2 to create formal links between the existing regional and national ecosystems that provide complementary capabilities, **allowing the SMEs to take advantage of new opportunities**. In fact, through the network, this will give – especially for the "More-than-Moore" domain – a say to the SME community which currently cannot afford the costs of a voice in the determination of nanoelectronic development policy. **The ecosystem would foster a true "open innovation" model for RTD in Europe**, allowing the rapid development of new companies through spinouts from universities, institutes and large companies, the reduction of "closed innovation" risk for all companies, the opportunity for large companies, and venture investors, to benefit through the company growth and exit though IPO, trade sales etc. and for companies to grow through acquisition.

ENI2 will impact the human capital for nanoelectronics in Europe by hosting young scientists and forging closer co-operation with the Universities aiming to create content and disseminate methodologies well matched to the skills needed by the rapidly-evolving nano-electronics industry. On a wider level, the socio-economic impact of ENI2 will be to position Europe as a major player in research, development and innovation, able to master innovative micro/nano technologies in order to use them into systems. In addition, by intensifying the research efforts and by involving all the players throughout the value chain, it will be possible to spur the development of innovative silicon solutions and to strengthen the position of European firms in the global market. The proposed infrastructure will also be instrumental **to keep and foster competitive manufacturing facilities on the European ground.** On the other hand, the **New Members States** (NMS) countries enjoy a considerable research potential allowing for R&D at low TRL stages, strengthened recently thanks to the Structural Funds based investment.

Nevertheless, continuation of the development at mid-TRL is difficult due to lack of adequate facilities, thus, limiting attractiveness of the research for industry.

Share of hi-tech products in the NMS industry is much below EU average. Reduction of this gap is crucial to improve EU cohesion and stability of the EU economy.

ENI2 intends to have an important impact on strengthening innovations in NMS through guiding the research towards well-chosen directions, harmonized with the European nanoelectronic ecosystem effort, facilitating access of NMS researchers and industrialists to the leading edge European R&D centers and in consequence, **improving integration of the NMS industry at the European level**. On the other side, it is expected, that the ENI2 strategy through strengthening collaboration within a well-defined nanoelectronic ecosystem, will facilitate collaboration of the NMS research teams with EU15 industry, thus building mutual trust, allowing for inflow of fresh ideas and solutions.

ENI2 integrating the nanoelectronic research ecosystem across all Europe shall make efforts to remove or at least considerably decrease existing barriers.

By addressing in a coherent and complementary way the three pillars of Horizon 2020, ENI2 will contribute directly in achieving some of the objectives of the Digital Agenda of Europe 2020.

8. Long-term strategic Programs

The Joint R&D&I Long term Programs will be submitted to the European Commission and the National Public Authorities for endorsement, reflecting the medium-term **commitment** and the involvement **of both Member States and the European Commission.**

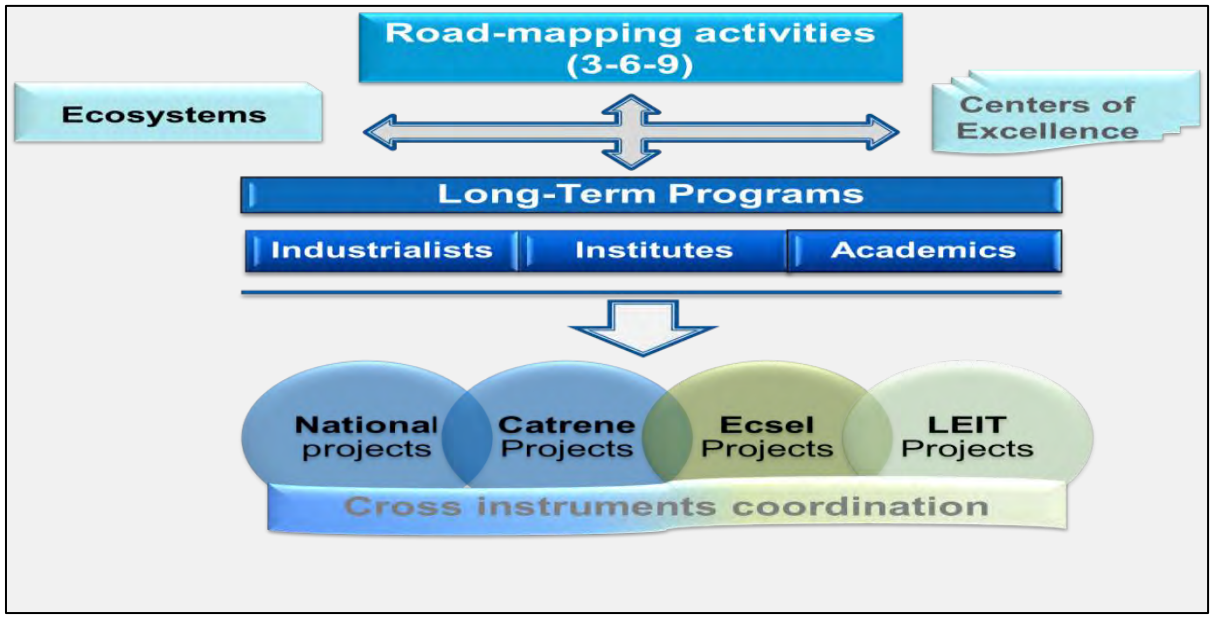
Each Program is relying for its execution **on an adapted Infrastructure** grouping the key European players identified to take the lead in this domain and focus the adequate resources.

It is planned to discuss and align the Strategic long term Programs with the Public Authorities and the European Commission to achieve the required approvals. Each Program will rely on an adapted Infrastructure reflecting the involvement of each Member State. The project must encompass the 3 R&D horizons. This means 3 subprojects. We will use 3 years as the unit of time for each horizon. Each level of the infrastructure is leading one of the subprojects. But each level can participate to all subprojects; it is a cooperative endeavor.

Each subproject is divided into Work Packages lead by an appropriate competence center.

The project should address the relationships with the SMEs and involve equipment makers.

Long term Programs (3-6-9 years) may therefore best be viewed as technical domain of activities (projects), each addressing a well-defined area of research and each (financially) responsible only for this topic. To ensure coordination between related topics, the overall technical domain co-ordination will be performed by an ('umbrella") independent body, responsible for Steering of the Domain Program and Co-ordination



of all inter-project activities within this domain; the Cluster Steering Council (CSC). Through this operation, the CSC will effectively integrate related subjects over a far larger area than could be performed within one 'umbrella' only.

As the program as a whole may be running under different funding schemes and regulatory regimes (National, EUREKA, EC), financial tracking of projects will be performed by the specific body or program. Should arbitration be required for situations within a project, than again this will follow the relevant rules. The CSC will be advisory in such matters, if so required.

The CSC consists of Public Authorities and core members of the most important contributors to the overall program being both technically and logistically selected for this council. On relevant matters, this council may be extended with the project leaders of the different projects and/or observers from the (technically/financially) contributing parties. This to act as a further means for ensuring compatibility with the goals and liabilities of the organizing 'umbrellas' and other 'stake holders' in the particular R&D area. In this way, the CSC may also serve to be a technical consultancy and advisory body for future programs.

In a separate document, and as an example, we have detailed the content of a Multi-year program addressing the NANOSCALE FET domain.

Annexes

1) Expression of interest forms

ENI2 is an open and living initiative. Based on questionnaires, as shown with the following "ENI2 expression of interest form", detailed input was and is collected and consolidated for e.g. the "Smart Energy", "Smart Sensors" and "3D Integration" domain.

ENI2 Expression of Interest form

Smart energy Areas of collaboration	Potential contribution Yes/no	Priority level (*)
Materials and Processes		
New materials for high Power semiconductors (SiC, GaN, Saphir, Diamond…) and associated manufacturing processes (Homo-hetero-localized epitaxy, characterization and test…)		
On SOI medium power technologies		
Low power Mixed analog technologies		
Low power RF technologies		
New materials and associated processes for Smart derivatives compatible with power		
New materials for large passive capacitors and inductors (high power, high frequency…) used together with semiconductors in power conversion		
Logic with HV applications and embedded flash: shrink path & HV properties (40….100V)		

Smart energy Areas of collaboration	Potential contribution Yes/no	Priority level (*)
Power production technologies		
300mm power production (process, metrology, materials, infrastructure)		

(*) Priority 1 to 3. 1 is the highest

ENI2 Expression of Interest form

Smart Sensors Areas of collaboration	Potential contribution Yes/no	Priority level (*)
eHealth sensors/actuators		
-Bio Sample Preparation *oxide functionalization for very efficient and reproducible bioprobe binding*		
- Micro pumps based on piezo-electric materials		
- MEMS based fluidic actuators		
- Fully electronic detection after PCR *APS architectures with capacitive or NW sensors*		
- Drug delivery: e.g. micro pump for insulin, micro needle, etc.		
ePaper: LCD, touch screens on plastic, etc		
High efficiency image sensors – *UV/Blue on SOI or 3D RGB on SOI*		
High efficiency solar *PV cells embedded below SOI CMOS chips*		
Gas detectors, e.g. MEMS based electronics nose *UCL – metal oxides on heating membranes, coated NW, metal oxides for water vapour*		
Novel materials and new functionalities – on-chip antennas –>metamaterials for miniaturization, high-Q passives for adaptation, MOSFET/control IC for reconfigurability and front-end/analog (especially Ultra Wide Band data transmission and RFID-type remote power sourcing); use of functionalised Silicon Nanowires or graphene sheet as sensing platform for gas sensors and/or biochemical sensors; Development of electromechanical lab-on-chip to study the coupled effects in thin films and nano-objects (nanowires, nanobeams, ...) such as the piezoresistance effects, magnetostriction, thermomechanical effects, ferroelectricity, flexoelectricity, etc. RF devices which use the electrical and mechanical properties of silicon to realise low power, high Q, highly reliable radio frequency capacitors and filters.		
Ad-hoc, faultless wireless connectivity coupled with smart sensors		

Other suggested collaboration areas
- Energy harvester; close on-chip circuitry to lower parasitics on-chip electronics with MEMS

ENI2 Expression of Interest form

3D Integration (1) Areas of collaboration	Potential contribution Yes/no	Priority level (*)
Through Silicon Via Technology		
Costefficiency of conventional drilling processes	no	
Alternative drilling and filling processes	yes	3
Materials research for reliability/lifetime *- a bunch of CNT (carbon nanotubes) in contact holes can be of interest for improving the vias in interconnection network, to facilitate the heat dissipation)*	yes	2
Thermo-fluidic-mechanical design and modelling *: impact of TSV on self-heating in SOI circuits*	yes	2
Research on influence of TSV on processed chip performance *– monitor stress creation with CMOS piezocircuits and impact on variability*	yes	3
Thin wafer/die handling		
Temporary carrier and die release during die-harvesting		
Improved P&P performance (accuracy, productivity)	no	
Alternative die manipulation mechanisms for fast and accurate placement	no	

Other suggested collaboration areas
– on-chip antennas =>metamaterials for miniaturization, high-Q passives for adaptation, MOSFET/control IC for reconfigurability and front-end (RF/analog, especially Ultra Wide Band data transmission and RFID-type remote power sourcing) - Energy harvester; close on-chip circuitry to lower parasitics

(*) Priority 1 to 3. 1 is the highest

2) Key Workshops

ENI2 KEY WORKSHOPS-MEETINGS		
Lyon	Concept elaboration	June 2, 2010
Brussels	Objectives definition	November 30, 2010
Dublin	R&D&I Infrastructure definition	January 12, 2011
Berlin	Kick-off	February 3, 2011
Paris	Smart sensors-smart energy	March 15, 2011
Cork	NanoscaleFET	March 24, 2011
Paris	Support Action structuration	June 23, 2011
Paris	Steering Group-General Assembly	September 26-27, 2012
Brussels	Heterogeneous integration	November 14, 2012
Berlin	Infrastructure	February 25, 2013
Paris	General Assembly	June 13, 2013
Grenoble	NanoscaleFET	October 1st, 2013
Brussels	Smart sensors	November 1", 2013
Paris	Systems Design	December 20, 2013

3) Identification of research facilities (Example)

PROCESSING

Main Equipments	Techniques/Competences
Si, Ge RPCVD	Nanowires growth
200 and 300 mm etching tools	Development of nanomaterials integration processes Nanopatterning and ultrathin layers etching
200 mm Nano-imprint	rapid and high resolution lithography
300 mm III-V (As and P based) deposition tool	III-V materials thin film growth
E-beam and DUV lithography, etching plasma tools, (flash- and thermo-) nanoimprint, , PVD, ALD, PECVD, CMP, ion implantation Deep RIE, vapor HF, supercritical drying, double-side lithography, wafer sealing Wafer sawing and wire bonding	Operation of a Renatech processing facility for the development of test structures for research purposes with MOS, NEMS and MEMS capabilities Wafers: size up to 100mm, Silicon, silica, glass, plastic
Commercial and home-made CAD softwares	Integrated Circuits design (CMOS, BiCMOS) Antennas design

CHARACTERIZATION

Main Equipments	Techniques/Competences
200 and 300 mm XPS	Surface chemical analysis
Probe stations: I-V, C-V, dc, ac, transients and pulsed Hall and magnetoresistance (up to 9T) 200 mm cryogenic probe-station (80K-350K) 300 mm low noise probe station	Electrical characterization, low-frequency noise Parameter extraction: transport, interfaces quality
AFM with EFM, C-AFM, TUNA, MFM with x-y-z feedback closed-loop with environmental control	Near-field morphological, electrical, mechanical and electro-mechanical characterization
3D interferometer/vibrometer	Static and dynamic topography of MEMS
Spectral reflectivity and transmittance using an integrating sphere	Characterization of optical properties (e. g. of materials for PV applications, PV cells)
Dark (fast or ultra-fast) transient I-V measurements Transient and DC I-V measurements under dark and illumination conditions Optical pump-probe spectroscopic measurements	RRT (Reverse Recovery Transient) for minority carriers lifetime measurement (PV applications) Conductance and photoconductance measurements Photoconductance decay for lifetime measurements

RF and mmW Vector Network Analyzer Spectrum analyzer RF Prober Anechoic chamber	Calibration, de-embedding Parameters extraction Antennas RF-MEMS

MODELLING

Main Equipments	Techniques/Competences
3D-2D-1D self-consistent home-made codes based on the Keldysh-Green's function formalism and atomistic empirical pseudopotential or k.p Hamiltonians.	Numerical simulation of quantum transport in nanostructures in the presence of elastic and inelastic scattering. Geometrical generation of random defects such as roughness, edge disorder, neutral and charged defects to address performance variability issues
Analytical models and home-made numerical methods based on Keldysh-Green's function formalism.	Modelling and simulations of scanning gate microscopy (SGM) experiments.
Atomistic description of vibration modes based on an extended valence force model, imported in home-made codes to address transport properties within the Keldysh-Green's function formalism.	Phonon dispersion curves and phonon transport in disordered or heterostructured nanodevices to evaluate their thermal conduction and thermoelectric performance
Diagrammatic technique to take into account different orders of the tunnel-coupling between leads.	Transport properties of the single-electron transistor tunnel-coupled to both normal and superconducting leads.
RF CAD: Circuit design and simulation (Agilent ADS), 3D finite elements software for electromagnetic simulations (ANSYS HFSS, CST Microwave, Sonnet, Agilent Momentum, ...)	Expertise in modeling and simulation results use Development of new modeling concept using TLM (Transmission Line Matrix)

4) Follow-up activities (Recommendations)

4.1 Roadmapping:

- Common needs on collaborative development have to be updated on a regular basis.
- Complementary analyses have to be conducted to identify critical applications and associated performances that will drive technological development.
- The initial first-cut provided by ENI2 in System Design and smart sensors must be reinforced to promote knowledge sharing and facilitate efficient collaborative actions.

4.2 Research Infrastructure

Based on the roadmapping activities and the corresponding contributions, the key Academic players have been identified in the ENI2 domains. A project could be proposed aiming to integrate the first level of the ENI2 infrastructure.

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