ENI² inputs to the H2020 ICT Work Programme 2016 – 2017

February 5, 2015

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Context

Unit A4 – Components has asked the ENI² community for inputs in the elaboration of ICT Work Programme 2016 – 2017. The present document is an answer to that request. It has been elaborated by the seven ENI² road mapping working groups :

- *Nanoscale FET*

Technologies, materials, device architectures, integration methodologies and processes for the continued shrinking of horizontal and vertical physical feature sizes to reduce cost and power consumption, and to improve performance

- *Smart Sensors*

Smart Sensors are systems which include a measurement chain (sensor + analogue conditioning electronics + processor + transceiver) and a power distribution chain (battery/energy scavenger + power management)

- *Smart Energy*

Technologies, materials, integration methodologies and processes for the realization of more energy efficient devices and systems

- *Outside System Connectivity*

Technologies needed to connect most elements of the internet of everything (IoE), covering both RF/mmW (wireless or wireline) and optical interconnect technologies.

- *Heterogeneous Integration*

Technologies and design tools and methodologies for the integration of separately manufactured components that in the aggregate provide enhanced functionality

- *System design*

Technologies, methods and tools that enable semiconductor companies jointly with system solution providers and academic research centers to design innovative cost (production and ownership), energy effective, environment friendly, safe and secure solutions for tomorrow's silicon based systems.

- *Equipment and Manufacturing Science*

Production, metrology and characterization equipment supporting the large scale manufacturing of technologies, and tools and methods for fab productivity enhancement.

General introduction

The potential scope of research topics in Nano-electronics is huge, and beyond the capabilities of the European nano-electronics community. The ENI² ambition is to contribute to structure and coordinate R&D&I in Europe and thereby address fragmentation, avoid unnecessary duplication of effort, and identify and encourage new or hitherto uncovered areas of technology development. This is done in line with the recommendations of the ELG[1] for a "more focused support to R&D&I aligned to an agenda proposed by the industry". In particular, "normal calls in H2020 will focus on more exploratory research that will bring differentiating factors for the industry to compete on a global scale".

The ELG has identified three market opportunities that industry in Europe is well placed to capture, in order to raise European semiconductor production in line with market developments. These are:

1. the emerging markets for smart connected objects and the 'Internet of Things'
2. the vertical markets where Europe has clear strengths such as automotive[2], energy, medical and life sciences as well as security
3. the mobile convergence market

While those markets are very diverse, all underlying systems include a chain whereby some "information" is detected, analyzed, acted upon and transmitted. To power the system, a power flow co-exists in parallel to this data flow (see figure 1). This decomposition into generic functions provides a grid to analyze the future requirements, and to identify common requirements across many applications. In turn, those common needs can be translated into new technology requirements. Following this approach, the ENI² working groups have identified prominent topics to be addressed in the H2020 calls pertaining to the ICT Work Programme 2016-2017.

[1] A European Industrial Strategic Roadmap for Micro- and Nano-Electronic Components and Systems – Implementation Plan – June 2014

[2] Which could be extended to "smart transportation"

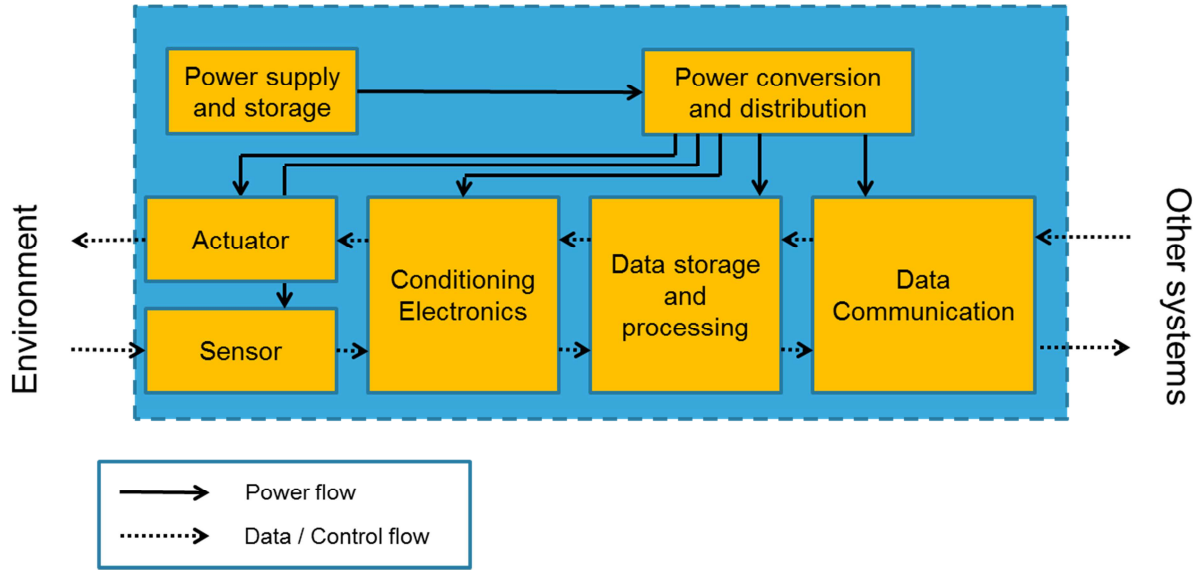

Figure 1 - Decomposition into generic functions of an arbitrary electronics system – depending on the system, some building blocks may be absent (e.g., sensors, actuators and conditioning electronics in a network router)

Section 1 : Nanoscale FET

The Nanoscale FET working group of ENI² covers the technologies, materials, device architectures, integration methodologies and processes for the continued shrinking of horizontal and vertical physical feature sizes to reduce cost and improve performance of the "data storage and processing" building block of any electronics system. The main topics to be addressed by H2020 ICT calls are the following :

1.1 Nanodevices in the ultimate More Moore and Beyond-CMOS domains:

- FinFET/Trigate/Ultra-thin films fully-depleted and fully-inverted MOSFETs with novel channels (Ge, III-V, 2D/TMDs) and gate stacks
- Lateral and vertical Nanowires with Si, strained Si and integration of alternative channel materials (SiGe, Ge, III-V, 2D/TMDs: HfSe2, ZrSe2, MoSe2/HfSe2 hetero-structures, etc.) III-V transistor (analog) on CMOS (digital)
- III-V transistor (analog) on CMOS (digital)
- Junctionless ultra-thin films, multi-gate MOSFETs and NW
- Small slope switches for ultra low power: Tunnel FET (integrability, complementary to CMOS), with Si, strained Si, alternative source/drain/channel materials /hetero-structures (SiGe, GeSn, SiGeSn, III-V, 2D) ; Negative gate capacitance FET with Ferroelectric materials
- Integration of novel high k dielectrics/metal gates with alternative channel materials
- Embedded memories (MRAM hetero-integration, Advanced RRAM physical and technological concepts)
- 3D sequential integration and design techniques for hetero-integration (including hetero-integration of advanced FETs with embedded memories: RRAM, MRAM...)
- Thermal management: impact on ultra-thin films and 3D integration

1.2 Novel interconnect architectures:

RC reduction : Nanowires, Carbon materials - nanotubes vias for reduced resistance, Airgap for ultimate capacitance. Material interface engineering offering to improve contact resistance and track resistivity.
Low cost electrochemical methods for materials deposition and integration in a flexifab.

1.3 Nanocharacterization methods:

including electro-thermo-mechanical-magnetic properties, reliability of novel devices and structures, extraction of parasitics, variability characterization : electrical and physical dopant fluctuation, metrology for materials and nanodevices.

1.4 Modelling and simulation of nanodevices:

including semi-classical, quantum, atomistic and multi-physics effects (thermal, mechanical, magnetic…), coupled materials-device simulation

Section 2 : Smart Sensors

The ENI² smart sensors working group focuses on the objects that acts as interfaces between the Internet and the "things" (which may be people, animals, machines, buildings, and also nature related objects as soil, rock, plant etc.…). In this paragraph, "smart sensor" also covers "smart actuators".
Those objects will enable

- The identification of the thing they are associated to. For instance, an RFID tag enables the identification of the things it is glued upon.
- To sense the parameters which characterize the thing. A sensor associated with the living room of building X will enable the measurement of its temperature.
- To act upon the object

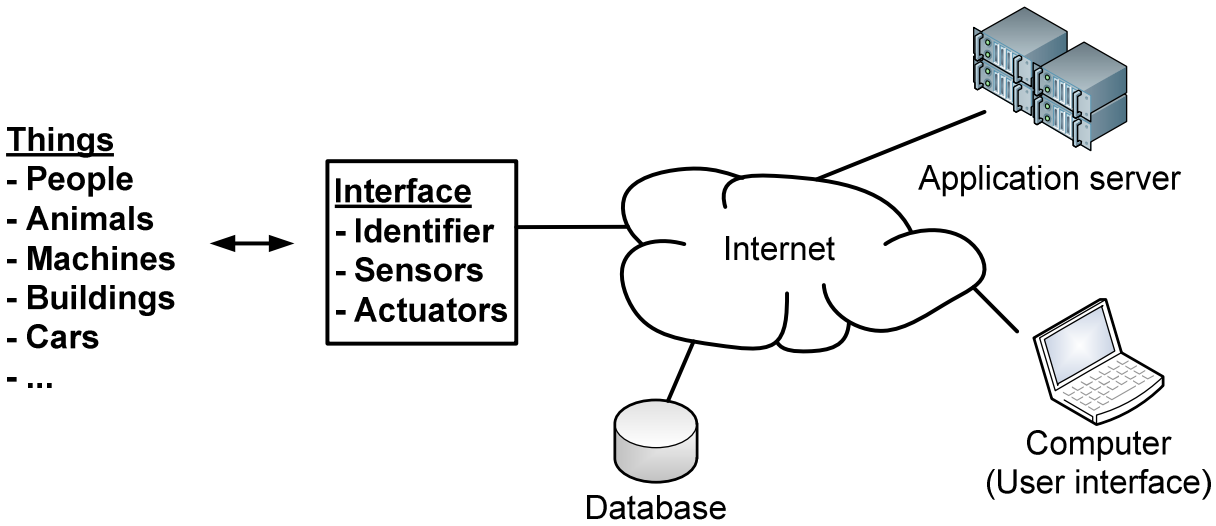

Figure 2 - Focus of ENI² "smart sensors" working group

The specific key building blocks of a smart sensor which are not covered by other ENI² working groups are :

- Transducers (CMOS sensors, gas, ultra-sound, micromechanical, optical, chemical and electrochemical, biomedical, biometric parameters, blood analysis…)
- Actuators
- Ultra low power transducer interface electronics and A/D converters
- Multifunctional materials and interfaces for advanced sensors

The main technologies to design and realize those building blocks are :

- MEMS / MOEMS / NEMS
- Printed electronics & batteries
- High sensitivity detection using Nanostructures and Nanodevices (nanowires realized with different materials, carbon nanotubes, 2D layers, etc....), and more generally integration of sensing functions / structures / materials on Si
- Functional packaging (e.g., micro-fluidics)

- Modeling, simulation & characterization

Whatever the technologies investigated, research projects in smart sensors must result in progress along at least one of the following "requirement classes" while not degrading the other ones.

Requirement classes	Topics
Anywhere (at any physical location)	Miniaturization and integration, integrating with textiles, implants (biocompatibility), harsh environment…
Autonomy (no human intervention)	Low-power consumption (consuming nothing when doing nothing). Energy scavenger & storage (zero power concept)
Low cost	Modularity, re-use, initial/incremental cost…
Sensing anything	New sensor, improved precision, sensor fusion (aggregation of heterogeneous sensors), algorithms…
Connected	Integration in local networks or in the IoT, Security & Privacy

Section 3 : Smart Energy

The ENI2 Smart Energy Roadmap has the ambition **to ensure the European technological capabilities to achieve the EU targets for 2030**: share of renewable energy in the electricity sector would increase from 21% today to at least 45% in 2030, (*1 - COM(2014) 15 final – A policy framework for climate and energy in the period from 2020 to 2030, Brussels January 2014*), the greenhouse gas emission reduction target for domestic EU emissions of 40% in 2030 relative to emissions in 1990 and the Commission's analysis shows that a greenhouse gas emissions reduction target of 40% would require an increased level of energy savings of approximately 25% in 2030.

In the **vision of ENI2 Smart Energy the enablers** achieving the ambitious energy related targets are **in all application fields generating, distributing and consuming electrical energy** and in the ones **where the use of electrical energy could substitute classical approaches** as mechanical, hydraulic or combustion driven actuators.

European leadership in the related ICT technologies is an essential base for European competitiveness in the application areas like energy management, automotive, industrial drives, health care and lighting.

This means that on European level in the area of ICT Key Enabling Technologies the following research activities have to be performed in the ICT program on the lower levels with specific focus themes as preparation for further broader research in the frame of the ECSEL JTI.

3.1 Compounds Materials / New Materials:

Scope:
Research on highest efficient power semiconductor materials for the next generation of converters or inverters.

- Medium TRL levels (short to midterm duration to market) for GaN on Silicon / Silicon Engineered substrates and on higher system voltage SiC based components;
- Lower TRL levels for other materials (e.g., Diamond on Silicon / Silicon Engineered substrates, low dimensional materials such as novel 2D materials and nanowires not covered by the Graphene Flagship project);
- Materials capable to operate in a "normally-off" mode are of particular interest, offering potential gains in terms of efficiency and footprint for most applications.

Addressed applications with the new materials are:

- DC/AC converters for solar power, AC/AC converters for Wind power: modules, switches, diodes, ICs supporting highest energy efficiency in power conversion
- DC- DC converters for direct DC use from wind or photovoltaic sources in the connected neighborhood (retail houses, manufacturing sides, office/large buildings)
- Highly efficient converters for all kind of bi-directional energy flow for intermediate storage applications
- Power switching modules in motor drive inverters
- Battery management and reverse protection
- Energy braking recovery system
- High efficiency power convertors for consumer applications
- High efficiency contactless/RF power transfer for consumer and automotive applications

Impact:
Building a European supply chain for technologies that would enable 50% reduction of energy losses, a 30% reduction in form factors and reduction in the total count of components and of peripherals in the conversion applications.

3.2 Integration of Intelligence and Power

Scope:
Research on intelligent and smart power applications, impacting both consumption and management of energy and power in both high power and lowest power applications.

Addressed applications by the integration of intelligence and power are:

- High voltage smart switches for grid coupling and energy transport in AC/DC/DC/AC for HVDC (High Voltage Direct Current)
- Smart grid monolithic AC switch with high galvanic isolation, very low R_{on}, self-powered, over current, voltage, temperature protected, full control and status indication, communication
- Energy scavenging systems (heat/light/vibrations/RF), incl. wireless energy transfer, for self-powered sensors.
- Advanced energy storage with 3D or 1D micro/nano battery materials for integration with energy harvesting. Energy storage in a hybrid system for integration with harvesting and to support energy provision during periods of intermittent harvesting.
- power management IC, building and street parameter sensor (temperature, pressure, humidity, light, windows and doors position, chemicals, air quality, human presence, human activity…)
- Lighting applications
- Smart plugs
- Smart energy breakers
- Smart patches
- DC bus systems with intelligent controllers and switches
- Electric drivetrains in conventional applications (including smart transportation)

Impact:
Controlled distributed systems with close to zero on-site maintenance efforts based on secure ICT systems with lifetimes fulfilling industrial requirements, enabling reduced overall energy consumption. Enabling technology for the Internet of Things, including regarding form factor requirements' (e.g., 1 cm^3 form factor).

3.3 Packaging

Scope:
High temperature capable packages serving new materials and 3D technologies with lifetimes fulfilling highest requirements and the integration capabilities for new kind of different interface conditions.

Impact:
Leverage of the advantages of new technologies like GaN on Si, SiC, or others due to higher temperature capabilities and enabled industrial use by high efficiency, long lifetime and high reliability.

3.4 Processing

Scope:
Processing capability for new materials and new technologies related to power semiconductors – lower TRLs in institutes, medium TRLs first capability in industrial environment.

Impact:
Transfer of small scale technological advantages towards manufacturability with knowledge regarding wafer volume scale manufacturing aspects.

Section 4 : Outside System Connectivity

This section lists the main research topics addressing the development of the capabilities needed to connect most elements of the internet of everything (IoE). This includes supporting connection of a broad range of sensors, devices, products as well as datacenters and to support information processing and analysis for many applications (i.e. mobility, energy, health, and others) with RF/mmW (wireless or wireline), optical and radio over fiber (RoF) technologies. The technological implementation of data security and integrity during transmission are within the scope of this section

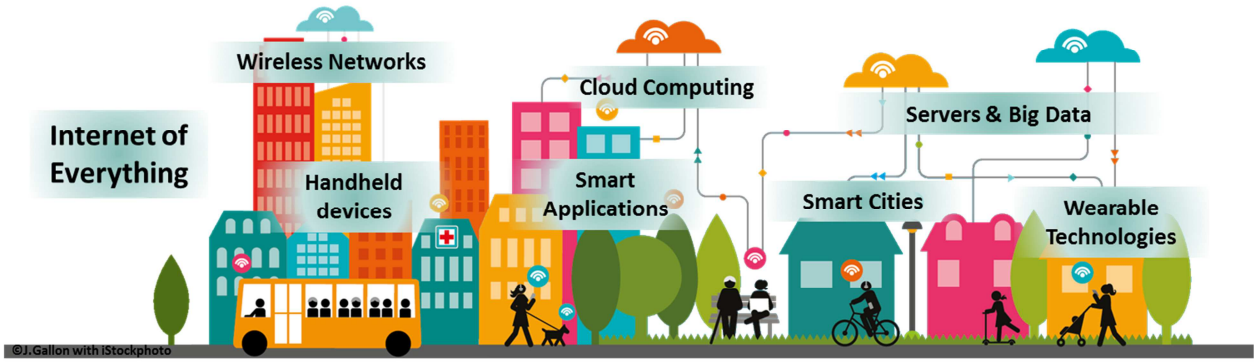

Figure 3: Of Things and Humans: "Impact of connected smart devices will add $1.9 trillion to global economy, disrupt every aspect of business, by 2020", said GARTNER in 2013 (graphic arts: courtesy J.Gallon for CEA-Leti)

According to CISCO, by 2018, 80% of the data traffic might be produced by datacenters-to-datacenters connections or inside datacenters, especially due to increasing cloud computing. Moreover, IP traffic traffic (e.g. involving a terminal access) would be more than 60% produced by wireless connections (fixed-Wifi or mobile).

A strong double-trend emerges: low power and integrated technologies, initially required for access components, clearly enter now in infrastructures. At the same time, high data rate and versatility which were supported by infrastructures belong now to terminal access components properties. This trend forces to overcome the historical skills and technologies partitioning.

In order to sustain a cost effective and energy saving deployment, we need:

- On the one hand, to push existing Wireless RF & mmW, Wireline mmW, RoF and Photonic technologies to their limits through smart design know-how and to tune these technologies to the edges,
- On the other hand to produce technology breakthroughs, by exploring lower TRL approaches on materials and structures (e.g nitrides, oxides etc.) enabling the scalable fabrication of reliable devices with a f_{max} in the THz range.

Accordingly, the "Outside System Connectivity" work group identified the following main targets which will transversally appear in a wide range of applications, ranked here from access to long haul, and according to the datarate:

I) RF/mmW Wireless technology & design for access & short connections:
- Innovative ultra-low power components for IoT and M2M
- Handheld devices technologies
- Integrated and smart antennas

II) RF/mmW Wireless & wireline technology & design for infrastructure:
- Highly integrated and cost effective solutions for small cell
- High speed (>10 Gb/s) and cost effective backhaul and fronthaul
- Radio over fiber for "last mile" and electro sensitive environment

III) Optical/Photonics technology & design (including packaging for electro-optical integration)for high speed link:
- Cost effective 40Gb/s to Tb/s silicon photonics enabled solution for data center & cloud computing
- Tb/s system for long haul

Involvement in standardization process, which tends to fix the hardware functionalities for a long time, is also crucial to guide technological developments. Moreover, these efforts should go with related design and test automation methodologies, to ensure optimized time-to-market.

Section 5 : Heterogeneous Integration

The "Heterogeneous Integration" working group investigates technologies and design tools and methodologies for the integration of separately manufactured components that in the aggregate provide enhanced functionality. Therefore, while there is also heterogeneous integration at the chip level (e.g. logic and HF ; logic and power), it is not addressed here but by the "System Design" working group.

Heterogeneous systems integration is an overarching topic for research which is related to all of the other themes and its presence is clear in all of the areas encompassed by of this document because every system has numerous different components and they all need to be connected together in an effective and cost efficient manner. However, there are some issues which need to be addressed regarding the motivation for the use of wafer scale and SiP or SoC technologies. The choice of which approach to adopt needs to be informed by comparative studies as well as a cost/benefit analysis of the different technologies available. The reliability of these new approaches needs to be addressed and design tools made available for the creation and evaluation for 'application specific assembly scenarios'

Systems level Integration Technologies encompass :
- 3D Integration Interposer/ Smart Interposer
- 2D Flexible and wearable electronics
- Design Tools (Co-design of heterogeneous smart systems including 2D, 3D and packaging integration)

Proposed Topics for H2020 ICT Work Programme 2016 - 2017:
- Demonstrate the merits of 3D integrated system over 2D SoC
- Develop reliability models visualisation techniques and lifetime projection models for 3D IC
- Create a 3D foundry and develop design tools and PDK for 3D systems design and manufacture
- Closing the power chasm between what can be generated and what is used in an autonomous sensor system
- Development of low power multisensor Systems
- Large scale deployments of low power autonomous multi sensor systems for monitoring large populations (e.g environmental monitoring or tracking farm animals)
- Flexible and wearable sensor systems, embedded memories on flexible substrates for wearable electronics
- New and Heterogeneous Materials Development for harsh environment devices
- Reliability and the development of new tools for the evaluation of integrated systems
- Establishment of models for lifetime prediction in heterogeneous systems

- Packaging technology for SiP sensor and actuator systems addressing contact/separation dilemma of integrated Smart Sensor Devices.
- Design methods to ensure electromagnetic compatibility of heterogeneous devices at IC, package and board levels.
- Development of smart sensor systems for biomedical applications (e.g. smart catheters for minimally invasive surgery, probes for deep brain stimulation)
- Organ-on-chip (e.g. for medicine development and screening, human disease modelling)

Section 6 : System Design

System design looks at the technologies that will enable to overcome the design challenges due to the ever increasing complexity and heterogeneity of embedded systems, which require designing System-on-Chips integrating IPs and subsystems realized in digital, analog, high voltage, software etc...

The most important challenges identified are :

- Increase of complexity and heterogeneity, requiring the use of several specialized design platforms and tools and methods to accelerate the simulation in order to perform the larger number of verifications
- Extremely low power or zero power system design, requiring tools to evaluate the power consumption through all design phases
- System oversizing due to the lack of tools to perform large design space exploration given the huge number of parameters to be considered
- Define adequate architectures (many-cores, multi-processing, cache coherency, etc…) to support software driven systems
- Abstraction levels description / modeling:
    - Due to the heterogeneous domains which need to cooperate together, it is extremely difficult to have the same level of abstraction (models) between all of them
    - There is a lack of standards addressing the interactions between domains, models and tools
    - Interoperability between models coming from different sources

These challenges need to be solved under stringent constraints of productivity and efficiency in terms of design performances and quality.

For productivity, the vision is that people, in the future, will no longer capture the specifications through drawings and “Word” documents, but through executable models, moving to languages such as UML. Towards that vision, the working group has identified three main research areas:

- Executable representation of system functionality & extra-functional properties modeling (e.g., power consumption, timing, memory bandwidth, etc…) to be available from the early design stages
- Verification & validation of the system performance by the introduction of parallel simulation
- Design productivity by defining and developing the right standards to ensure operability between IP and subsystems to maximize reuse

In these three domains, there is a need for European cooperation to propose inputs for standards.

For efficiency, circuit and systems solutions need to be aligned with technology solutions. Additionally circuit and system technology solutions need to be aligned with applications. The key concept is meeting performance objectives (including security, weight and power requirements) by exploiting tradeoffs between applications, circuit/system design and fabrication technology through a global integrated design process (co-engineering methods and tools) taking into account security and SWAP – small weight and Power – requirements). An additional benefit accrues from automation or semi-automation of this global design process, but the crucial part of the definition is concurrency: developing system, circuit and technology at the same time on parallel paths. The combined system/circuit technology solution required for next generation high performance products represent a multidimensional optimization process that can optimize several factors in concert to achieve a better solution, ultimately leading to extremely integrated system.

Section 7 : Equipment and Manufacturing Science

7.1 Providing sustainable solutions for the Factory of the Future

2016-17 Specific challenges

As European Fabs are characterized by lighter investment, smaller structures and legacy software and equipment, they need to be flexible and agile. Generic standards have to be defined in order to facilitate the global integration for future virtual factories and to facilitate the access to new comers (solution providers).

Programs will have to be defined to address both the area of open and standardized production data exchange and also enabling factory systems with enhanced security. Given the level of complexity of the ecosystem to be built, knowledge management and sharing will be instrumental and developments will have to be fully supported.

Another aspect to address is the definition and standardization of an intelligent data integration and visualization as well as intuitive and safe human-machine/robot interaction. This is an essential precondition for creating a maximum added value for humans in the production as the most agile element in the factory of the future.

Sustainability should also be further developed at environmental level : new methods and solutions should be further developed or demonstrated for manufacturing application.

Proposed Topics for H2020 ICT Work Program 2016 - 2017:

- Standardization of production flows and data – definition of standard flows and diagrams for the manufacturing of semiconductor components
- Supply chain integration – to streamline the production of complex products (systems on chip, multi-module packaging, etc.) through virtual fabs
- Standardized ontologies for big data – to boost product learning curve and facilitate the entry of new solution providers
- Toward the “App’s” world – evolving from todays’ legacy systems toward connected and secured individual / portable applications.
- Multi-modal interaction modalities: definition of standard flows and diagrams of innovative control and interfaces for collaborative human-machine/robot interaction.
- Towards the Green and sustainable manufacturing fab – to push energy consumption improvement, to develop methods and tools to support sustainable fab environment, to reinforce and develop innovative security system and methods, and sustainable methods and tools for operators confort

7.2 Dynamic Knowledge Management: raising engineering know how to the next level

2016-17 Specific challenges

When deploying innovative solutions in the field of Manufacturing Sciences, several challenges have to be addressed. First of all, the management of the existing legacy in terms of equipment, processes and systems is today a major concern when considering the ageing workforce.

Then, the introduction of new concepts, such as predictive techniques and operational research will require the extension of the traditional engineering perimeter and the removal of barriers today existing between the various actors involved in semiconductor manufacturing.

Proposed Topics for H2020 ICT Work Program 2016 - 2017:

- Capitalization and sharing of the knowledge generated from concept and experience. It includes predictive techniques and process, but also smart evolving process.
- Dynamic management of a coherent knowledge “pedestal” for engineering – designing new forms of collective action, allowing to solve “continuous crises”

- Lifelong training of the engineer- how to continuously acquire the knowledge and competences required for a global / holistic product approach
- Networking and security in a moving environment with multiple and interacting knowledge fields (i.e. high diversity of technologies, products, resources, design and production context)

7.3 Developing new equipment capabilities

Most of the research avenues described in the previous sections (nanoscale FET, smart sensor, new materials for smart energy, etc …) will need new concepts, advanced R&D and innovation up to complete demonstration in manufacturing environment in the equipment field. This includes of course process equipment, but also metrology and characterization equipment. Some European equipment suppliers are world champions in their domain, and public support to maintain or even gain market share in that segment of the nano-electronics supply chain is essential.

R&D needs for the development of a full fledge process equipment go beyond the scope of H2020 LEIT programs. However, the investigation of new physical effects to achieve a process or metrology step, or deep understanding of the physics inside a machine, can be the subject of a smaller size collaborative R&D project.

An essential step to achieve availability of state-of-the-art equipment provided by innovative EU equipment suppliers is to foresee, in the new Work Program, a support to bridge the gap from equipment R&D to novel equipment assessment accessible for all EU players. The combined efforts, resources and expertise in a joint assessment of novel equipment for key enabling technologies will allow to foster and accelerate the successful transfer of novel European equipment into the world-wide market.

On top of the continuation of Semiconductor Equipment Assessment projects, proposed topics for H2020 ICT Work Program 2016 – 2017 are**:**

- Multi-physics simulation of process steps (e.g., plasma etch)
- 3D manufacturing process steps like conformal material engineering, atomic layer or selective film deposition on high aspect ratio structures
- Advanced metrology (3D, contamination , including advanced software and data treatment..)
- Advanced packaging equipment, in particular for heterogeneous integration

Appendix : List of contributing research institutions and companies

III-V Lab, France
Adixen Vacuum Products, France
Alcatel-Lucent, France
CEA-LETI, France
CNRS, France
Edacentrum GmbH, Germany
Fraunhofer-Gesellschaft, Germany
IMEC, Belgium
Infineon Technologies, Germany
Ion Beam Services, France
Italian Institute of Technology, Italy
ITE, Poland
KTH Royal Institute of Technology, Sweden
Micron Technology, Italy
Newcastle University, UK
NXP Semiconductors, The Netherlands
Philips Research, The Netherlands
Politecnico di Torino, Italy
STMicroelectronics, France
Thales Communications & Security, France
TU Delft, The Netherlands
Tyndall National Institute, Ireland
University of Oslo, Norway
University of Siegen, Germany
VTT, Finland