2A702: NanoTEST (NanoTEST)

EDA FOR SOC DESIGN AND DFM

Partners:

AMIS
CEA-LETI
INESC
Infineon
LIRMM
Philips
Q-Star Test
STMicroelectronics
Tecmic
Temento
TIMA

Project leader:

Erik van Geest,
Philips

Key project dates:

Start: January 2005
End: December 2008

Countries involved:

Austria
Belgium
France
Portugal
The Netherlands

The microelectronics industry is rapidly entering the nanotechnology era with circuit nodes well below 90 nm. Mass production is only economically feasible when the proper test technology is in place to reduce costs, improve quality and cut time to market. It is therefore essential for European chipmakers to develop new in-house tools and proprietary test methodologies in addition to the mainly US-sourced commercial test tools. NanoTEST will ensure development of the tools and standards for system-on-chip and system-in-package technologies. Availability of the right methods and tools earlier than for US and Asian competitors will contribute significantly to commercial success in Europe.

Manufacturing testing has become a major concern in the microelectronics industry as costs continue to expand, claiming an increasing percentage of total device manufacturing cost. In the period 2005 to 2008, 65 nm CMOS technology will be used for production and 45 nm technology will be developed.

As documented in the International Technology Roadmap for Semiconductors (ITRS), these technologies impose challenges on test methodology, triggered by an increasing number of gates per chip, smaller dimensions and new defect mechanisms. This is a real challenge, since the complexity of test generation grows exponentially with the number of gates. It will not be possible to achieve a high test coverage and fast ramp-up at acceptable cost with today's test methodology. This is confirmed by the MEDEA+ Electronic Design Automation (EDA) Roadmap, which identifies nine areas for test innovations.

European microelectronics companies AMIS, Infineon, Philips and STMicroelectronics intend to strengthen and realign the efforts they already put into testing in MEDEA+ phase one projects. They will build on the results of the MEDEA+ T101 TECHNODAT and A503 ASSOCIATE projects for a new MEDEA+ project: 2A702 NanoTEST. In addition to the four European chipmakers, this project brings together four research institutes and three SMEs. The composition of the consortium ensures efficient knowledge transfer from academic research and industrial research and development (R&D) down to production level in, for example, the STMicroelectronics/Philips/Freescale (formerly Motorola) 'Alliance' fab in Crolles (FR), Infineon fabs in Villach (AT) and Corbeil-Essonnes (FR), Philips fabs in Nijmegen (NL) and Caen (FR) and the AMIS fab in Oudenaarde (BE).

Meeting industry demands

Microelectronics system manufacturers impose tough quality requirements on chipmakers, even while technology nodes are still maturing. Common quality requirements are lower than 100 ppm, while actual manufacturing yield is typically lower than 90% — equivalent to 100,000 ppm.

Testing plays an important role in meeting quality requirements. On one hand, testing filters out defective parts,

allowing the enabling technology to bridge the gap between manufacturing yield and quality requirements. On the other hand, testing provides feedback on weak spots in the design and process. This is an emerging role of manufacturing test. It provides fault identification to support faster ramp-up. Not only are system-on-chip (SoC) devices and their building blocks addressed but also heterogeneous systems such as system-in-package (SiP) or possibly including micro-electro-mechanical systems (MEMS).

The MEDEA+ consortium will benefit from European co-operation by sharing results between research institutes and industry as well as between the large firms and with SMEs. As a combined force, the consortium has more influence with automated test equipment (ATE) and electronic design automation (EDA) vendors and in global standardisation initiatives.

NanoTEST will address completely new test challenges but will also further extend still immature methods explored in previous projects to enable their full exploitation in products.

Three work packages

The project will directly contribute to the commercial success of the European microelectronics industry in applying new wafer and packaging technologies, targeting not only SoCs but also SiPs. It will create breakthroughs in testing in the area of cost as well as achieved quality and time-to-market. The activities are split into three discipline-orientated work packages addressing technology, design-for-test and testing procedures.

This will result in:

- **Reducing the cost of testing during production by a factor of ten** by developing new methodologies that enhance tester throughput and reduce tester resources: for example, multi-site testing, low-cost test cells, advanced test interface boards and test resource reduction by on-chip test provisions that go much further than current design-for-test practices. A key factor is to determine the optimum balance between on-chip test provisions and off-chip test equipment. There is a growing market trend towards heterogeneous systems, such as SiPs, in situations where this is more economical than a single SoC. This project also intends to reduce the production test costs for SiPs. Issues to be addressed include test provisions for intra-package access and inter-die testing, wafer probe technologies, signal integrity issues affecting tests and the development of standards.
- **Improving the quality of testing**, despite the fact that occurrence of new defect types in 65 and 45 nm will initially drive defect levels upwards. This will be achieved by developing test methodologies for new defect types, as well as extending use of tester data into the domain of fault diagnosis for fast production ramp-up, characterisation and self-repair. Synchronisation fault test strategies play an essential role in covering new defect types. The work on diagnosis will provide the necessary feedback to zero-defect programmes driven by the automotive sector.
- **Speeding up the complete design-for-test and test program generation flow by a factor of ten** through re-use at the optimum abstraction level. At the same time, new methodologies will be developed for future designs containing, for example, globally-asynchronous/locally-synchronous circuits, volatile and non-volatile memories, radio frequency (RF), mixed analogue-digital signal blocks and sensors. Tools will also be developed to automate mixed-signal test specification and test program generation.

Ensuring European success

This project supports European efforts towards a leading position in microelectronics and the commercial success of the 65 and 45 nm technology nodes. Designs in those technologies will not only contain CMOS logic but also memory, mixed analogue-digital signals and RF, using process options. This project is indispensable to design and manufacture complex products in a short timeframe at market-compliant cost.

The European chipmaking companies involved in NanoTEST are all highly active in the consumer electronics, automotive and telecommunications sectors. The main competitors are the microelectronics companies from outside Europe, mainly from the USA and Japan. In these targeted areas, the growth in SoC will continue in a cost competitive environment. Furthermore, these sectors will lead in applying SiP. The test technology developed in NanoTEST will be a key contributor to the future commercial competitiveness of the European microelectronics industry and to the generation of high level jobs in Europe.

MEDEA+

MEDEA+ Office
33, Avenue du Maine
Tour Maine-Montparnasse
PO Box 22
F-75755 Paris Cedex 15, France
Tel.: +33 1 40 64 45 60
Fax.: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

EUREKA Σ!

MEDEA+ Σ!2365 is the industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.