MEDEA+

PROJECT PROFILE

2A704: Robust design for efficient use of nanometre technologies (ROBIN)

EDA FOR SOC DESIGN AND DFM

Partners:

CISC
CWS
Edxact
Hirex
Infineon Technologies
Philips
STMicroelectronics
Uni Marseille

Project leader:

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Key project dates:

Start: January 2005
End: December 2008

Countries involved:

Austria
France
Italy
The Netherlands

Modern system-on-chip designs show a strong trend to lower voltages and higher frequencies, while miniaturisation introduces new risks of signal voltage distortion with a resultant impact on performance. To reduce repetitive design activity and avoid unreliability or failures in service, the MEDEA+ ROBIN project aims to prevent these effects early in the design process. This is vital to improve circuit robustness and efficient use of production equipment in Europe. It will accelerate access to new chip technologies in key public sectors such as telecommunication, transportation and health care. And the resulting yield improvements will have a positive influence on costs and speed deployment.

Integrated circuits (ICs) may malfunction due to distortion, attenuation or delay of the signal waveform. It is therefore desirable that such issues are addressed early in the design stages of high speed digital circuits to avoid failures arising during laboratory work or – even worse – in the field.

Consequently, three major European semiconductor manufacturers decided to co-ordinate their R&D efforts by addressing a set of specific issues – including inductive effects, substrate noise, voltage drop, electrostatic discharges and radiation-induced errors – at design level. Additional expertise is provided by a laboratory with extensive expertise in quantum physics and five computer-aided design (CAD) and computer-aided engineering (CAE) companies.

Optimising trade-offs

The goal of the MEDEA+ 2A704 ROBIN project is to get the best results from currently available 130 and 90 nm and future 65 and 45 nm technologies by defining optimal trade-offs between circuit robustness in terms of yield and reliability, and efficient use of technology in terms of performance, density and power consumption. The ROBIN project is following a bottom-up approach, from technology to chip level, and then to package level.

Two major obstacles have to be circumvented:

1. Under design – not taking adequate account of physical effects when designing a chip, or considering them too late in the design process; and
2. Over design – introducing excessive design margins that hinder the optimal use of technology.

Macro-level couplings – that is power and substrate effects – and micro-level couplings in terms of signal interference are also being addressed. Most of these issues concern effects at die level and in systems in packages (SiPs). Low-cost manufacturability is also being taken into consideration.

ROBIN is driven by constraints from areas such as ultra-low power for portable applications at Philips, SiP projects such as circuit designs for mobile phones at Infineon and non-volatile memory (NVM) at STMicroelectronics. Time-to-market will be shortened as a result of the reduced number of redesigns – with less 'wrong go/no go' effects during the sign-off process – as well

as more efficient technology data management and improved failure diagnosis. The main actions consist of increasing the expertise of partners in analogue circuit theory, building repeatable models, designing test structures, confronting simulations and measurements, defining 'go/no go' flags for manufacturing and, finally, drafting design rules that guarantee proper chip functionality without excessive pessimism.

Improving design sign-off

Design sign-off includes verification that all functional, timing and power requirements are met. Currently, achieving design sign-off is a time-consuming – although non-exhaustive – activity for 130 and 90 nm circuits. Designs all too often pass traditional verification checks, yet fail at silicon level. This forces design teams to resort to costly diagnosis and repair methods such as the use of electron beam or focused-ion beam techniques.

The situation is expected to worsen for the next generation of 65 and 45 nm technology nodes. Every time the circuit clock rate doubles, crosstalk intensifies by a factor of two, while dynamic power net deviations attributable to voltage drops will significantly influence circuit supply voltage, so causing unpredictable circuit response and overall design failure.

Current approaches to voltage-drop issues consider this effect either at the register transfer level (RTL), which is too early for accurate grid sizing, or as a post-process of the graphic data system (GDS), where it is too late to make changes without costly redesign. The cost of repairs will therefore increase, together with the associated delays and mask costs for silicon re-spins.

Consequently, preventive methods applied in a wholesale fashion – such as increased timing margins or physical guard banding – will increase design and manufacturing costs, leading to larger, costlier dies and suboptimal performance in the final silicon device.

Even simple, passive elements of a high-speed design – the wires and the chip packages themselves – will make up a significant part of the overall signal delay, causing glitches, resets, logic errors and other problems. Massive parasitic data will have to be stored and processed to uncover subtle nanometre effects in large designs.

Current solutions available on the market are mainly from the USA. These commercial tools already suffer from limitations, while evidence of their future development is very limited.

Complementary approaches

The MEDEA+ framework makes it possible to tackle the problems involved from different angles. ROBIN is complemented by another MEDEA+ project: 2A701 PARACHUTE – parasitic extraction and optimisation for efficient microelectronic system design and application.

Both these MEDEA+ projects incorporate work on the analysis of parasitic effects on electronic circuits. However, while the analysis of parasitic effects and a robust design are inherent to ROBIN and PARACHUTE, the former contributes to the design flow in a bottom-up approach starting with the nano effects in modern chip technologies, whereas the latter takes a top-down approach to researching the topic from systems level.

Facing up to competition

Leading companies in the USA have developed and are regularly upgrading their own internal solutions for statistical timing analysis; this capability gives them a significant edge on global competition in terms of sign-off signal integrity analysis. The inclusion of statistical timing analysis and process variation modelling among the MEDEA+ project topics will make a positive contribution to helping European semiconductor companies achieve a more robust sign-off methodology.

SiPs are gradually penetrating the chip market. A number of companies are now offering CAD tools that mainly address printed circuit board (PCB) designs. Silicon chip designs with the focus on sub-65 nm structures are not well covered or at least only provide a view of problems that need to be addressed.

The results of the MEDEA+ ROBIN project will ensure that European chipmakers can improve circuit robustness and make efficient use of production equipment to face up to global competition. CAD and CAE partners will largely benefit as well, as the outcomes of the ROBIN project will enrich their product and services portfolios.

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