PROJECT PROFILE

2A718: Tera-scale multi-core processor architecture (TSAR)

EDA FOR SOC DESIGN AND DFM

Partners:

ACE bv
Bull S.A.S.
CEA-LETI
Compaan Design bv
FZI
NXP Semiconductors
Philips Healthcare
Thales Communications
TU Delft
Uni Leiden/LIACS
UPMC/LIP6

Project leader:

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Key project dates:

Start: June 2008
End: May 2011

Countries involved:

France
Germany
The Netherlands

TSAR focuses on the design and use of many core, tera-flop architectures for high-performance computing. The project will extend the performance envelope established with multi-core homogeneous processor architectures and their associated memory models to support a wider spectrum of synchronisation and locking granularities. This enables the creation of the next generation of powerful, larger scale parallel computing devices together with the software and tools to support their exploitation. The outcome will be solid foundations for, and an enhancement of, the European semiconductor industry on the world stage, resulting in considerably increased market potential and employment opportunities.

There is an ever-increasing demand from consumers and businesses for high performance computing ranging from medical imaging and scientific computation – such as in bioinformatics, electromagnetics and astrophysics – to financial analysis, real-time data mining and artificial intelligence applications.

These high-performance computing (HPC) applications all have in common not only a critical need for the fastest possible speeds for program execution but also superior data throughput and the capability to aggregate substantial distributed computing power. This is challenging the information technology (IT) industry to deliver tera-ops – trillion operations per second – performance and terabytes of bandwidth.

With the end of uni-processors with faster clock rates, performance scaling is now taking an irreversible step toward parallel architectures. Life after Moore's law is another Moore's law predicting a doubling of parallelism per work load every two years.

High-performance platforms

The MEDEA+ 2A718 TSAR project is focused on the design of many-core architectures targeting tera-scale performance. It is addressing both hardware and software techniques that support parallel computing while adopting a number of guiding principles such as the priority to solve the combined power/memory/instruction-level parallelism (ILP) walls, the consideration of a variety of computing models, the cost of designing at 65 nm feature size and below and the leverage of software as producer, but not consumer, of performance gains.

The numerous development challenges include: network-on-chip (NoC) based shared memory architectures scalable up to 4096 cores; innovative design and validation of in-network cache-coherence; task parallelisation and optimal mapping of applications on Kahn process network (KPN) based streaming structure; virtual prototyping and field-programmable gate array (FPGA) based prototyping of large systems; and software development including operating systems (OS) for optimal many-core compilation targeting both streaming and shared memory models.

Key targets of the TSAR project are to:

- Design and validate – in terms of functions and performance – different versions of the TSAR cache-coherent non-

uniform memory architecture (ccNUMA) machine;
- Provide a design flow to optimise parallelisation and map automatically applications on streaming architectures; and
- Demonstrate the proof of concept on both virtual prototypes and FPGA-based platforms.

The ultimate goal of this MEDEA+ project is to provide high-performance, scalable many-core platforms to encourage the research and development (R&D) community to develop add-ons and/or port their applications onto such platforms

Innovative approach

TSAR project partners have considerable experience in related topics and in the participation in European projects, particularly in MEDEA+. Moreover, the involvement of three systems companies and two small and medium-sized enterprises (SMEs), both electronic design automation (EDA) software tools suppliers, supports the ecosystem for the European nanoelectronics industry.

In comparison with many other European initiatives set up in response to the same challenge, as exemplified by the French System@tic/Ter@ops or the FP6/hArtes projects, TSAR has its own specific. One of the main differentiating factors of TSAR is the ambition for a large-scale cache coherence and memory consistency. In addition, the two main parallel architecture models – respectively shared memory and streaming models – are addressed in the project at both hardware and software levels while sharing design and prototyping methodologies.

This openness and the completeness of the work bring TSAR strategy closer to the Research Accelerator for Multiple Processors (RAMP) initiative led by the University of California Berkeley in the USA and involving many academic and industrial partners on the same topics.

Divide and conquer

TSAR proposes adoption of the so-called 'divide-and-conquer' strategy in the design of new multi-processor architectures. This involves distributing concurrent operations across many small processing units.

The integration of a high number of processor cores in future chip architectures requires the development of innovative solutions to solve many issues. These include memory access, distributed cache-coherence protocol, architecture design, and software portability and optimisation. TSAR will bring new European techniques together to provide a scalable solution.

By addressing the development of basic multi-core processors, the MEDEA+ project intends to secure European competitiveness in many industrial sectors such as computing, medical imaging, automotive, mobile communications and multimedia. A successful position in these markets is strongly dependent on the design productivity provided by the availability of core components such as processors.

Range of results

At the end of the project, TSAR is expected to exhibit two main outcomes:

1. Many versions of a ccNUMA machine with different protocols and associated architectures; and
2. A compilation flow supporting the automatic optimisation and mapping of applications onto streaming architectures.

These two realisations will be able to execute real-life applications for demonstration.

Access to the virtual prototype of the TSAR ccNUMA machine will be made available to the R&D community in order to motivate and encourage their development of add-ons and porting of applications for evaluation.

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