PROJECT PROFILE

# A511: Tools and methods for IP (TOOLIP)

**DESIGN METHODOLOGIES**

**Partners:**

Bull
CEA-LETI
CNM-IMSE
Design & Reuse
Deutsche Thomson Brandt
Empolis Knowledge Management
Infineon Technologies
ISD
KORG Italy
Philips Semiconductors
Sci-Worx
SIDSA
Siemens
STMicroelectronics
Thales Communications
Thomson Multimedia
TILAB
University of Ancona
University of Bologna
University of Karlsruhe (FZI)
University of Madrid
University of Paderborn

**Project leader:**

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**Key project dates:**

Start: January 2001
End: December 2003

**Countries involved:**

France
Germany
Greece
Italy
The Netherlands
Spain

**Dramatic improvements in process technologies are permitting integration of complete systems on single chips (SoCs). This has stimulated the explosion of small, mobile devices that provide advanced communications and information capabilities in consumer appliances, automotive electronics, networking and industrial automation applications. Despite their complexity, SoCs must be delivered very rapidly to decrease time to market. The MEDEA+ TOOLIP project addresses European producers' need to employ reusable intellectual property (IP) cores, system level modelling and verification techniques, and a seamless design flow that accepts existing and emerging tools, as the means of meeting these demands.**

Today's home appliances and teleworking tools are becoming increasingly complex, requiring ever-higher levels of system integration for the implementation of cost effective novel services such as video-on-demand and remote health monitoring. Similarly, in automotive multimedia accessories, many functions must be integrated in order to save space and cut costs.

An obvious way to reduce time-to-market for new system generations is, wherever possible, to reuse – possibly with adaptions – the IP inherent in the designs of existing modules. The application of reuse methodology for SoCs has already proved its validity by bridging the productivity gap, meeting critical time-to-market objectives, reducing costs, reducing design errors, and easing verification and testing.

Quality is becoming a decisive factor in the IP business. Customers often distrust the suppliers due to earlier bad experiences. Moreover, the difficulty in obtaining IP that exactly matches users' needs often prevents a deal. In order to facilitate and spread reuse in industry, the MEDEA+ A511 TOOLIP project is therefore concentrating a major effort in the area of IP qualification and customisation.

## Cost-effective approach

Several attempts have previously been made to define standards and guidelines that guarantee IP quality through their construction but they have lacked truly practical applicability. In fact, system-level design – and especially SoC development – requires new concepts for the automation of enhanced platform-oriented design flows extending from system level to layout level.

TOOLIP does not seek to introduce a new language or a new set of tools that force industry to invest a large amount of capital and time. Rather, it proposes IP management methods, tools and standards that are currently missing from the system design chain, and which will guide the system architect in choosing the best cores for any given system.

A major contribution is the creation of a seamless environment supporting IP reuse through a rich, standardised platform that implements multiple levels of abstraction. This will allow hardware/software co-design, and make it possible to integrate and provide interoperability between state-of-the-art tools for IP management, checking, selection, modification, validation and simulation.

A close relationship between leading chip manufacturers and systems houses in the consortium of the three-year project will facilitate the reuse of IP from key domains such as broadband communications, multimedia, processor cores, and small offices and home offices (SOHO). Their participation, together with electronic design automation (EDA) companies also ensures a market orientation, and enforces synergetic effects.

Several planned demonstration platforms will focus on relevant developments defined by the industrial partners, involving SoC integration of large and complex designs.

## Multiple aims

The initial aim of TOOLIP is to offer a specification of reuse-oriented requirements permitting the intra- and inter-company exchange of qualified IP. The consortium is also exploring ways to simplify the definition of the correct interface for a variety of current and future bus standards and processor architectures in order to simplify the design of IP for external use. And, as typical IP design involves partitioned elements fleshed out by geographically dispersed teams, the partners are using the Internet as their medium for communication.

Existing catalogues often provide only static navigation structures or simple, relatively ineffective text-based syntactic search functions. Therefore one of the goals of TOOLIP is to introduce efficient query functions that identify the best-suited IP and thereby save time and money during the subsequent design phases.

Despite the existence of various IP providers in the market, the selection process for users remains complex and time consuming. TOOLIP will encourage efficient IP integration by offering methods and tools that are supported by the providers, yet can be customised to users' needs.

Validation and distributed simulation techniques under development are aiming at solving existing interoperability and large-scale performance evaluation problems. In addition, the project is introducing flexible parameter formats that allow application-specific customisation by the IP provider, or design adaptation by the IP user.

## Fully documented design flow

A design flow for complex SoCs must meet stringent requirements, such as a high degree of IP reuse, optimal hardware and software partitioning, concurrent flow of software and hardware development, and efficient parallel or distributed co-simulation and co-verification introduced early in the design process. Using a highly distributed simulation engine, the open unified platform proposed within TOOLIP will fulfil these criteria and allow simulation of IP cores developed with different tools and methodologies.

Thus, the project's overall objective is not to provide just another simulation tool, but a fully documented design flow with recommendations and guidelines based on emerging state-of-the-art development tools, and acting as an additional layer of abstraction between the available tools and the system.

To achieve this target, an extension of a system specification language (such as SystemC) is being developed. New features, new semantics, and new mechanisms for performance estimation of factors such as delays, throughput, and power consumption will have to be added.

In parallel with the definition of innovative methods and tools, a second important area of activity is monitoring and actively participating in defining and influencing international standards governing inter-company IP reuse. The contribution of European industry will directly influence the success of products and tools in the market. Furthermore, the interaction between large European companies within a common project will accelerate this necessary IP exchange between companies.

## Essential for success

IP reuse and IP exchange constitute one of the most challenging aspects of electronic design innovation. They are essential if tomorrow's large-scale devices are to be designed with decreased time to market, with high system reliability and reduced overall cost. The adoption of best practices, as proposed in TOOLIP, will enable European industry to secure and safeguard leadership in the key markets of Internet, digital consumer electronics and wireless communications.

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