



T30I: 0.1 μm fabrication engineering (0.1 μm Fab)

OTHER EQUIPMENT

Partners:

40-30
Air Liquide
Alcatel Vacuum Technology
ALES
ALTIS
Faure Ingénierie
GRECA – Uni. Grenoble
INCAM
LETI
Mondia Quartz
Philips
RECIF
SEPREX
SOPRA
STMicronics

Project Leader:

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Key project dates:

Start: January 2001
End: December 2004

Countries involved:

France
Italy
The Netherlands

The growing complexity of integrated circuits and the trend to build complete system-on-chip (SoC) architectures are placing demands on semiconductor manufacturers to provide ever tighter incremental gate spacing. The MEDEA+ T30I 0.1 μm Fab project brings together leading European semiconductor manufacturers and their equipment and material suppliers to develop fabrication technologies for the reliable production of silicon chips with next generation feature sizes down to 100 nm and below. The project is split into two parts to cover improving material purity for the next two generations of IC technology and developing relevant hardware to be used with the new production materials.

Integrated circuit (IC) technology is steadily moving to increasingly smaller feature sizes to offer microelectronics users more functions at lower price. With decreasing device dimensions, however, the sensitivity of devices to small defects and impurities caused by the production process increases. Many new materials, such as high- and low-dielectric constant (k) materials and copper interconnects, will be introduced in process technologies for 100 nm and below. These require development of new or improved cleaning gases and chemicals and it is essential to investigate to which kind of defects these materials are sensitive. New sources of contamination may become dangerous, such as molecular contaminants from the air that had no negative influence at larger feature sizes.

On top of these problems, there is a steady pressure to invent and develop methods to save energy and deionised water, and to develop methods to improve environmental, safety and health aspects in a wafer fab. The MEDEA+ T30I 0.1 μm Fab project brings together most of the European expertise on advanced semiconductor fabrication engineering to tackle these problems. It supports efforts to strengthen the leading

position of European gas and chemical companies and the development activities of the many small and medium size enterprises (SMEs) collaborating in this project on related equipment for wafer cleaning, photo resist stripping and prevention of particle and molecular contamination. The project will increase collective know-how and allow each partner to be more efficient in its specific domain.

State-of-the-art in Europe

The International Technology Roadmap for Semiconductors (ITRS) stated in 2001 that a new technology would be introduced every three years but leading IC chipmakers have introduced a new technology every two years or even less to maintain their share of the market. In general terms, Europe is at the state-of-the-art in IC manufacturing. In order to keep this position, they need a continuous supply of state-of-the-art gases and chemicals preferably from local – that is European – suppliers.

Europe also needs to work on contamination control to have the necessary yield to be able to manufacture the complex designs that will be required. This makes it

necessary to identify potential contamination sources and to understand the possible impact of various contamination species on processes and on yield.

Contamination control may be achieved by prevention, through the application of new fabrication engineering and equipment designs, or by improved wafer surface preparation. This includes optimisation of promising building blocks, such as dilute RCA recipes, ozonated chemistries and the development of new clean and dry concepts, as well as the integration of these building blocks into an appropriate surface preparation process-flow. This improved surface preparation makes high demands on the purity of water and chemicals, and on wet cleaning equipment.

Defectivity a major concern

Defectivity is a major concern in the transition to more aggressive technologies. Innovative ideas are required to decrease the number of particles present or generated in the equipment and it is necessary to reduce contamination of the silicon by various gas compounds in clean-room air. This last point is especially critical for 65 nm technology.

The major cleaning equipment competition lies in the USA and Japan. International Sematech also started evaluation in 2001 of photo resist stripping with supercritical CO_2 , which is an important task of T301. Europe is leading on defectivity for the advanced vacuum line.

Molecular contamination has been a worry in Japan because the factories there are located in areas with high sulphur concentrations – near volcanoes or big cities. Therefore Japanese companies are

ahead in detection and prevention of molecular contaminants.

For example, chemical vapour deposition (CVD) of the order of 15 nm is a method of getting a uniform copper film on sidewalls and bottoms of vias and trenches. The mainstream technology for completing copper deposition is electro-chemical deposition (ECD). It is anticipated that this technology is capable of the feature size required for 0.1 μm technology, but new chemistry should improve uniformity and reduce defectivity.

Materials and equipment

The MEDEA+ T301 project is split in two subprojects:

1. A materials-oriented sub-project, which addresses materials with the level of purity required for 0.1 μm technology until 2002 and for 65 nm technology from 2003; and
2. An equipment-oriented sub-project to develop items of hardware too small to form part of a stand-alone project but which will be employed in close relationship with new materials used by semiconductor manufacturers.

Sub-project 1 is aimed at providing a European source of the promising gas and chemicals market required for 65 nm technology. It is addressing major issues and roadblocks listed in the ITRS for the front end of line (FEOL) and back end of line (BEOL) of a full silicon process.

Sub-project 2 encourages European SMEs to validate new concepts in the fields of wafer cleaning, photo resist stripping, particle and defect avoidance and supply management – where the focus will be on particles originating from new maintenance

kits or the pumping line – and molecular contamination, addressing the issue of adsorption of gas on the surface of wafers.

Securing competitive power

This MEDEA+ project is designed to secure competitive power in the European gas and chemicals industry sectors – both sourcing and distribution – as well as ancillary equipment. In 1999, the world market value of device manufacturing – CVD, deposition and etch – together with wafer cleaning and photo resists exceeded € 7.5 billion.

Currently, Europe is weak in photo resists, slurries for chemical mechanical polishing (CMP), liquid for ECD and precursors for CVD, and must improve this situation. It is anticipated that it is in the emerging markets area that growth will be the largest.

The largest gas and chemicals company has the technical and sales infrastructure ready for the exploitation of the results of the project while the numerous SME partners in T301 are also prepared. The French SME 40-30, for instance, has already started on a second production site specifically for the exploitation of the results.

Annual workshops will be organised to announce the results of MEDEA+ T301. This will be open to all potential customers, whether a partner in the project or not. Further to the necessary protection by patents, publication will be ensured either by the individual companies or as a consortium through the project leader.

The MEDEA+ T301 project is expected to make a significant contribution to European know-how, new business development and related employment.



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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.