PROJECT PROFILE

T302: Atomic layer deposition for 100 nm devices (ALAD1N+)

OTHER EQUIPMENT?

Partners:

ASM Belgium
ASM Microchemistry
IMEC
LETI
Philips
STMicroelectronics

Project leader:

Dr. Ir. Ivo J. Raaijmakers, ASM International

Key project dates:

Start: January 2001
End: June 2002

Countries involved:

Belgium
France
Finland
Italy
The Netherlands

As the scale of CMOS transistor dimensions shrinks to gate lengths of 100 nm and below, chip manufacture will require dielectric materials capable of being applied at very low thicknesses, while still minimising leakage current and giving good interfacing to other process layers. ALAD1N+ extends earlier exploration of a highly promising process allowing controlled deposition of atomic-scale multilayers with the necessary characteristics. The major European semiconductor manufacturers are participating in this research, because this MEDEA+ project will pave the way for the development of production-ready tools that will give Europe a valuable lead in future-generation chip fabrication.

Atomic layer deposition is a breakthrough technology for semiconductor manufacturing, permitting the deposition of very thin films. In contrast to conventional chemical vapour deposition (CVD), it enables successive monolayers to be added with precise compositional and thickness control, even over irregular underlying topographies.

ASM international, co-ordinator of MEDEA+ project T302 (ALAD1N+), is the recognised world leader in this technique, having already patented the process and aspects of the equipment, and marketing it under the name of Atomic Layer CVD™ (ALCVD™). Experimental systems were supplied to research partners IMEC and LETI at an early stage of the earlier MEDEA ALAD1N project, which successfully proved the feasibility of ALCVD processes for integrated circuit production.

The 18-month ALAD1N+ project forms a seamless continuation of R&D work started during MEDEA. As before, ASM Microchemistry and the ASM Belgium research laboratory, plus chip manufacturers Philips and STMicroelectronics continue to be members of the consortium.

The scope of the new initiative has been broadened to embrace three applications. Processes and equipment are being developed for gate dielectrics and gate electrodes, as well as for barrier and seed layer deposition in dual damascene structures of inlaid metal interconnects. Initial investigation of ALCVD processes for inter-poly dielectrics is also planned.

It was initially assumed that this type of process would become essential for the production of 100-nm devices. However, recent progress in conventional techniques makes it probable that large-scale industrial introduction of ALCVD techniques will be deferred to the advent of the 70-nm node in 2005. The fruits of the present research will thus provide Europe with a mature technology well in time to profit from the future market opportunities.

Improved process and deposition control

Atomic layer deposition differs from CVD in that the substrate is exposed alternately to separate gas-phase precursors, which each cover the substrate only by less than an atomic monolayer. In conventional CVD, two gaseous species are present in the reactor at the same time. Consequently, the new

ASM ALCVD process permits the build-up of a series of atomic monolayer deposits in a well-controlled manner. Deposition conditions can be optimised for each individual precursor, and the gas flow maintained for long enough to ensure that a uniform chemisorbed layer coats the whole surface, even at the bottoms of deep trenches.

Early results from stand-alone equipment have demonstrated a unique ability to produce dielectric oxide layers with equivalent oxide thicknesses of around 1.4 nm and leakage current less than $1x10^{-7}$ A/cm², which is many orders of magnitude below the allowable limit of 1mA/cm² for low power devices.

In current process flows, gate dielectrics of nitrided silica are applied in batch reactors, after which the wafers are transferred to separate reactors for deposition of the doped poly-silicon gate electrodes. Between these two steps, the dielectric is exposed to air before being capped by the electrode. This could cause the formation of additional interface oxide In ALAD1N+; the ALCVD reactor is therefore combined with other tools in a cluster fabrication system that enables the two steps to be effected without intermediate air exposure. In addition, the cluster can incorporate pre-cleaning and surface pre-treatment modules that render the wafer more suitable for monolayer deposition.

Another important issue is to minimise the migration of boron from the polysilicon into the dielectric. To solve this problem, the project is studying the use of materials with lower boron diffusivity than silica while maximising the dielectric constant (k). Testing of candidate materials and their evaluation as gate dielectrics in full CMOS process flows should be completed within the project period by the IC partners.

Solving interconnect scaling problems

Decreasing feature sizes require a corresponding scaling of interconnect densities – the number of layers will increase from the current six to eight or even ten in the near future. Because the vertical dimensions of the interconnect do not scale as much as the lateral dimensions, increasing aspect ratios create difficulties in the deposition of barrier and seed layers.

While the step coverage of today's physical vapour deposition (PVD) and CVD processes is inadequate to meet the need, that of ALCVD processes is close to ideal. This has been demonstrated by depositing conformal barrier films in very high aspect ratio trenches and vias with 100% step coverage.

Successful use of the ALCVD technique for 100-nm and smaller devices will require the integration of a suitable pre-cleaning stage in the cluster tool. Technology patented by ASM Microchemistry for chemical treatment at moderate temperatures (up to 400°C) is expected to offer a novel means of cleaning the damascene structures prior to metal deposition.

The consortium predicts that manufacturing-ready solutions for the manufacture of low-k/Cu dual damascene structures will exist by the close of the project, and that – from 2003 onwards – these could progressively replace conventional PVD and CVD for the production of barrier and seed layers.

Further innovations

Another area of interest is interpoly dielectrics, used as barrier layers to ensure charge retention in non-volatile memories. Here too, the current mode of manufacture is a two-stage process, whereby top and bottom electrodes of doped poly-silicon are added in a separate batch reactor. This method is incapable of providing adequate device performance at layer thickness below about 13 nm – and no alternative is as yet available for sub-100-nm chip generations, which require thicknesses of 9 to 11 nm.

ALAD1N+ will ascertain whether using ALCVD high-k materials, either alone or in combination with standard dielectrics, could provide the answer. A subsequent challenge will be to develop a cluster tool for deposition of the various layers, again without exposure to ambient air between successive steps.

Overall, industry has high expectations of the project. It has already enabled the consortium to develop new ALCVD material structures, and is establishing a strong patent-protected position for Europe. Both Philips and STMicroelectronics aim to adopt the technology – and Infineon has also expressed interest in participating.

The emerging innovations will assist ASM in becoming a major equipment supplier to the global marketplace. And the institutional partners IMEC and LETI will be able to use the acquired knowledge to pursue further avenues for the integration of atomic layer deposition into semiconductor technology.

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