T303: Contactless anneal and silicides system (CLASS)

PROCESS EQUIPMENT

Partners:

ASM International
ASM Belgium
LETI
IMEC
Schunk Kohlenstofftechnik
STMicroelectronics
XYCARB

Project leader:

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Countries involved:

Belgium
France
Germany
Italy
The Netherlands

As semiconductor manufacturing technologies advance, traditional approaches to annealing the wafers used in chip fabrication plants are approaching their technological limits. The partners in the MEDEA+ T303 CLASS project are developing a prototype wafer annealing system that is a radical advance on existing processes. The new system offers faster heat-up and cool-down rates and allows the precise temperature control of wafers during processing. This innovative technique will boost the skill and production capabilities of European integrated circuit manufacturers, their suppliers and the research institutes, and help them meet the chip manufacturing challenges of the 21st century.

Wafer-fabrication plants have been searching for methods of exactly controlled heating and cooling of wafers ever since the first integrated circuit (IC) was manufactured. Now the partners in the MEDEA+ contactless anneal and silicides system (CLASS) project are exploiting a new method of rapidly heating and cooling of wafers that is a major advance on existing methods.

The project partners are working on a newly developed rapid thermal processing system. This tool combines a number of novel features such as very fast heat-up and cool-down rates with simplicity of operation, high wafer throughput, excellent temperature uniformity and low power consumption. Three types of processes are targeted: annealing of shallow ion implants ('spike annealing'), annealing of silicides and rapid thermal oxidation.

Floating wafers process

Traditionally, three main systems have been used for annealing wafers during chip manufacture:

1. Conventional furnaces, with process durations of one to two hours;
2. Rapid furnaces, in which one or two wafers are placed close to a hot element that provides faster heat-up rates; and
3. Lamp-heated systems, in which high-intensity light sources are used to heat up the wafers very fast.

All three types suffer from disadvantages. Conventional furnaces are losing ground due to cycle time requirements, while the widely used lamp-heated systems put great demands on temperature control. On top of that, it is difficult to cool down the wafer rapidly after the annealing process is completed; a higher cooling down rate is necessary, especially for spike annealing.

With the new approach, the wafer is floating in between and in very close proximity to two hot massive blocks kept at process temperature. The blocks are perforated with many narrow channels through which gas flows such that a gas bearing is realised in which the wafer floats in a stable way without ever touching the blocks. In this case, the heat transfer from the blocks to the wafer is extremely efficient, resulting in heat-up rates exceeding 300 and 900°C per second when using nitrogen and helium, respectively. When the blocks are sufficiently thick, a uniform temperature across the wafer is guaranteed. The temperatures of the blocks will not decrease much with the heating of individual wafers. This means that only a simple temperature control is required.

The system uses exactly the same principles to cool down the wafers. After annealing, the wafers move between two water-cooled blocks, floating on the nitrogen or helium gas cushion to maintain a precise distance between the blocks. Cool-down rates are in the range of 200 and 600oC per second, respectively, again unusually fast.

Heating and cooling of the wafer through conduction rather than radiation, makes the heat transfer far easier to control precisely.

In addition to rapid heat-up and faster cool-down, the overall heating efficiency of the system is also superior to alternative systems. With the new system, up to 65% of the heating power fed to the blocks heats the wafer. By comparison, lamp-heated systems typically reach an efficiency of only 5 to 10%.

In addition, as the risk of temperature overshoot is much reduced, only a simple temperature control system is required. This is a real advantage over lamp-heating systems that often require complex temperature control.

Strengthening IC manufacturing

The primary goal of the CLASS project is to strengthen the production capabilities of the partners of the CLASS project, and support European development capabilities in new IC manufacturing processes and related equipment. The results of the project will drive new equipment manufacturing activities, as well as bringing a boost to European IC supplier industries. The research community will also benefit from participation in developing new ways of chip manufacture.

Detailed targets include:

- Achieving single-wafer processing throughput exceeding 160 wafers per hour for a two-module system, which is substantially faster than that of competing systems;
- Attaining uniformity levels of 0.5% in oxidation and 1% in implant annealing applications. Achieving these values is essential for future technology nodes;
- Significant reduction in operating costs by developing simplified heating systems, simpler temperature controls and reduced energy consumption – target energy consumption is 6 to 20 kW for a 300-mm wafer system, compared with 250 to 350 kW for competing lamp-based platforms; and
- Reliable implementation of spike annealing for the formation of ultra-shallow junctions, made possible by the much faster heat-up and cool-down rates.

Prototype development

Since the project commenced at the beginning of 2001, project partner ASM has developed and refined the prototype system, and has also shipped a further two prototypes to research institute project partners LETI and IMEC to enable work to proceed in tandem.

While the system is already capable of handling 200-mm diameter wafers, work has commenced on developing its capabilities for 300-mm wafers to meet IC industry demand. Successful manufacture of 300-mm wafers in a wafer-fabrication plant makes it possible to produce more than twice the number of ICs per wafer compared with 200-mm versions, for the same investment in staff, machines and floor space.

The system is already capable to achieve the technological requirements of a 130-nm CMOS process, now the standard for most wafer-fabrication plants. Additional development is already under way for manufacturing of 100-nm devices, the expected technology standard in the near future.

CLASS project partners consider this solution as having an built-in advantage in meeting future market needs for systems able to process single wafers in a technologically advanced and cost-effective way. It is expected that more and more new applications for single-wafer annealing systems will appear, for example for copper and low-k annealing.

In addition, the benefits of fast heating and forced cooling make the system ideal for spike-annealing applications, which depend on very fast heat-up and cool-down. The characteristics of the resulting ultra-shallow junctions are at the known theoretical limits of the annealing process.

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