PROJECT RESULT

Technology platform for next-generation core CMOS process

MEDEA+

2A703: Network-on-chip design driven by video and distributed applications (NEVA)

Novel circuit architectures for data-stream applications

An increasing number of processing blocks and memories have to operate in parallel and exchange data on-board the chip. To meet the demands of data-stream applications such as video, traditional silicon architectures are nearing their limits. Participants from across the industry combined in NEVA to develop innovative approaches to design, focusing especially on network-on-chip devices able to handle multiple processors and asynchronous circuitry. The project resulted in new design techniques for circuits able to manage data-stream processing that are already being used by major European chipmakers.

Electronic devices are becoming so complex – already a billion transistors per circuit by 2008 – that the integration potential of traditional bus-based silicon chip architectures is pushing the limits of feasibility for commercial applications.

Traffic jam in view

As a result, the alternative approach of asynchronous circuit design is now being re-examined for its potential in network-on-chip (NOC) circuit designs. Asynchronous circuit designs often have more flexible and robust synchronisation and communications mechanisms, while making it possible to reduce power consumption.

At the same time, systems-level mock-ups addressing a communications-centred design can offer formidable opportunities. Configurability techniques and compilers also have to be adapted to take into account new complex instructions that will help software and hardware resources fit together.

The MEDEA+ 2A703 NEVA project investigated the potential of such techniques in chip design. NEVA focused on NOC designs that make use of multiple processors and asynchronous circuitry, in particular for high-throughput video-processing and video-transmission applications subject to huge increases in data-processing demands as video applications become ever more ubiquitous.

Wide range of partners

NEVA brought together an unusually wide range of industrial and academic partners. The consortium aimed to develop innovative design techniques in three key areas:

1. Communications-centred design of NOC architectures using a high-level approach and transaction-level modelling (TLM) techniques, which are more and more accepted by industry;
2. Dynamic configurability to allow optimisation of resources at architectural and modelling levels, with a focus on new timing tools to improve reliability and compilers that are sophisticated enough to reconfigure hardware resources as necessary; and
3. Globally asynchronous locally synchronous (GALS) techniques for the implementation of asynchronous architectures, which would help deliver circuits with lower power consumption, as well as reducing clock distribution problems and associated speed limitations.

By the end of the project, the NEVA partners had achieved all their targets, producing 22 prototypes and 12 exploitable products in the form of models, software tools and design flows. The project results were demonstrated

using five different systems: a video-computing platform from NXP, high-definition TV (HDTV) from STMicroelectronics and three silicon circuits from LETI.

These outcomes have already proven of concrete benefit to the systems designers involved in the project. They have also had an impact on the design of a number of close-to-market applications, for example video-image filtering, MP3, multiple input/multiple output (MIMO), 3G mobile communications and multimedia streaming.

In addition, the partners produced 105 published papers, 4 PhDs and more than 7 patents.

Results already exploited

The industry partners, including more than 1,000 designers at STMicroelectronics, are applying the new tools and techniques gained from NEVA to internal projects, as well as to specific applications requested by customers. The electronic design automation (EDA) partners, meanwhile, have been able to extend their portfolio of products and services, and to commercialise new solutions on the open market.

NXP Semiconductors has for example developed four new products as a result of the project, STMicroelectronics has been able to produce six new products, while BULL and ACE have developed one new product each. Several partners have also been able to improve co-operation with others in the project.

Finally a huge standardisation effort was deployed by the project partners on the Open SystemC Initiative (OSCI) TLM standard. This defines application-programming interfaces (APIs) and a library that implements a foundation layer upon which interoperable transaction-level models can be built. The effort, which was led by STMicroelectronics, contributed greatly to the launch of the TLM standard 2.0.

Improved design tools

The experience of two partners in applying the techniques learnt within NEVA clearly shows the advances made.

STMicroelectronics can now benefit from a fully configurable compilation flow which is used by its product divisions. The speed of an MP3 decoder was demonstrated to be 30 times higher, without any transformation of the C source code. In addition, the activities carried out in NEVA by STMicroelectronics resulted in a prototype 45 nm node interconnection targeted at HDTV system-on-chip (SoC) devices, available on schedule with respect to the planned NEVA roadmap. This technique is immediately exploitable in circuits developed by STMicroelectronics for digital TV.

The NXP family of Trimedia very long instruction word (VLIW) digital signal processors (DSPs) is used in many media-processing products – such as digital TV, set-top boxes and similar applications that require H.264/MPEG-4 AVC video-compression encoding and decoding.

Based on its work in NEVA, NXP released an improved compilation system – the TriMedia Compilation System (TCS) 5.1 – in 2007. This provided high levels of optimisation. The certified Embedded Microprocessor Benchmark Consortium (EEMBC) benchmark score increased by more than 60% for the same silicon platform. Its successor – TCS 5.2 – supports the complete software development cycle: building a software component, navigating user-written code and compiler-generated intermediate files, simulating and debugging applications, analysing and tracking performance and code size.

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