PROJECT RESULT

Technology platform for next-generation core CMOS process

MEDEA+

2TI04: Device and circuit performance boosted through silicon material fabrication (DECISIF)

FDSOI to drive device architecture in the next miniaturisation nodes

Semiconductor designers and developers are forever seeking better solutions to meet market demand for higher performance at the same time as reducing power consumption. With recent advances in planar undoped channel fully depleted silicon-on-insulator (FDSOI) devices, many see FDSOI as offering a serious future alternative to bulk substrate technologies, especially at the 28 nm node and below – and even beyond the industry roadmap. The MEDEA+ DECISIF project worked on FDSOI, as well as other substrate and thin-film technologies, for CMOS applications which require both high performance and low power.

Consumers today want their smartphones to be able to access large files on the web, display high-definition video in real time and carry out fast processing for complex tasks. Not only do they want all this in a neat, small and battery-powered package but they also want never to have to recharge the batteries!

Within the CMOS community, ultra thin body (UTB) devices are becoming accepted as the most efficient way of improving circuit performance to meet such demanding user needs. Lower parasitic capacitances, higher performance and reduced power consumption are all characteristics of UTB architectures. The MEDEA+ 2T104 DECISIF project focused on generating an original UTB architecture based on advanced engineered substrates and other possible thin-film technologies.

The overall objective of DECISIF was to gather the main European actors in advanced substrates, integrated circuit design and manufacturing, and evaluate current substrate approaches and appropriate thin-film technologies for both high-performance and low-power CMOS applications. The emphasis was on integrating nodes of 45 nm and below.

FDSOI the way to go

The intention was not to develop new classes of substrate from scratch but to build on the results in materials and early devices achieved in the earlier MEDEA+ SILONIS project. DECISIF concentrated primarily on device and circuit demonstration including design, performance and yield, and on investigating the best performance/cost compromises for each approach.

Much of the project work was initially carried out at 45 nm. While emphasising device and circuit technology development, the MEDEA+ project also considered different substrate types as part of the project. For example, it examined use of strained silicon-on-insulator (sSOI) or hybrid-orientation silicon wafers as a means of boosting device performance compared with standard unstrained approaches.

DECISIF addressed five different families of wafers:

1. Thin silicon-on-insulator – SOI with thin silicon and thin oxide layers;
2. Strained SOI – SOI with a strained top silicon layer to enhance carrier mobility;
3. Direct silicon bonding (DSB) – hybrid orientation substrate, where a thin silicon layer is directly transferred onto the base wafer with no oxide layer in between;
4. SOI and bulk silicon substrates with active silicon layer orientation; and
5. SOI and bulk substrates with deposited epi-silicon-germanium (SiGe) layers.

The first step was the development of high quality and manufacturable sSOI substrates. However, during the course of the project,

advances in substrate manufacturing indicated that for extremely thin films, planar fully depleted silicon-on-insulator (FDSOI) devices had become a serious alternative to bulk technologies and partially-depleted technologies, especially at the 28 nm node level and below. FDSOI therefore became one of the key approaches investigated within the project for low power applications.

For the high performance domain, where PDSOI is an attractive option, DECISIF put emphasis on new flavours of engineered substrate such as SiGe channel and various crystal orientations of the top film.

Successful circuit demonstration

The project examined the FDSOI process compared with bulk silicon at circuit level. A test chip was implemented at 28 nm; this chip included a low density parity-checker commonly used in wireless applications. In addition, to assess the gain in performance, robustness, noise level and minimum working voltage of FDSOI technology compared with bulk ones, benchmarks were performed on high density SRAMs.

By the end of the project, DECISIF had successfully demonstrated the FDSOI approach on 28 nm SRAM using a substrate constituted of an ultra-thin silicon film on top of a thin buried oxide SOI. This arrangement allows back biasing of the transistor channel, giving a large degree of freedom to designers to implement low power design techniques.

As a result of the project, the DECISIF partners now see the FDSOI architecture as a potential approach for solving the performance gap at the 20 nm node compared with the objectives stated in the International Technology Roadmap for Semiconductors (ITRS). FDSOI has so far solved all the problems – channel electrostatic control and channel random dopant fluctuations – faced by the partners in scaling bulk transistors below 40 nm.

These FDSOI results will now be carried forward into a new CATRENE project – REACHING 22. REACHING 22 will make possible a design platform for 28 nm circuits using FDSOI transistor architecture, as well as evolving toward 22/20 nm. Another CATRENE project, DYNAMIC-ULP, has also started, targeting the demonstration of a complex system-on-chip device built with a 20 nm FDSOI technology.

Bright future

As regards industrial exploitation, project partner SOITEC achieved significant progress in the process control of extremely thin silicon film on thin buried oxide. As a result, the partners see FDSOI as a candidate for volume deployment of the architecture in future CMOS nodes of the ITRS.

Some industry observers see the FDSOI approach as having the potential to serve as a mainstream CMOS architecture down as far as the 15 nm nodes, where at present competing architecture exists such as the FinFET – a non-planar, tri-gate transistor built either on bulk or on an SOI substrate. The DECISIF partners believe that FDSOI is capable of taking chip designers and manufacturers a long way.

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