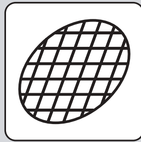
PROJECT RESULT



IC technology integration

MEDEA+

T206: CMOS SOI for low power logic and RF wireless (CMOS SOI)

Moving SOI digital, analogue and RF technology into the mainstream

The attraction of silicon-on-insulator (SOI) CMOS technology is growing worldwide for future 65 and sub-65 nm applications as a replacement for bulk CMOS to reduce power losses and increase speeds. The T206 CMOS SOI project demonstrated the technical benefits of SOI in logic, analogue and mixed digital-analogue applications as well as the growing importance of high resistivity SOI substrates for radio frequency (RF) applications. The experience gained by major chipmakers and their materials suppliers is helping Europe establish a strong position in this key technology for future volume products.

Silicon-on-insulator CMOS technology seems set to move rapidly from current niche applications in high speed computing to more general purpose volume use as SOI-based chips can function at significantly higher speeds than bulk CMOS while reducing electrical losses. The result will be higher performance electronic devices with much reduced power consumption, critical as device sizes continue to reduce.

An SOI device involves creating a thin layer of silicon on an insulating substrate such as silicon dioxide on the wafer used to make the integrated circuit. The transistor gate or switch junction is then formed above the insulation layer. Switching times are decreased due to the floating body effect and because drain junction and interconnection line capacitances are lower than in bulk CMOS devices.

In addition, there are no parasitic bipolars thanks to the SOI junctions, thus avoiding latch-up problems. And, as insulation is by shallow trench with the oxide layer ensuring all gates are fully insulated, wells are not needed and circuit density can be much increased.

Exhaustive evaluation

However, SOI is a relatively new technology, making it necessary to control a new process – though fully compatible with existing CMOS equipment – and to carry out electrical modelling to simulate and optimise devices. The MEDEA+ T206 CMOS SOI project set out to evaluate and compare the performance of partially depleted (PD) and future fully depleted (FD) SOI with bulk CMOS technology. FD SOI offers improved electrical characteristics compared with PD SOI and bulk CMOS, allowing optimisation for high temperature and extremely low voltage/low power applications, while PD SOI is optimal for high speeds.

The MEDEA+ project involved a balanced partnership from SOI wafer manufacturers to major European chipmakers, together with key research institutes and universities, involved in digital, analogue and RF application evaluation, device modelling and characterisation, and materials developments.

Work was split into three areas:

1. Low power digital, analogue, mixed and RF applications involving 130 nm PD SOI technology;
2. Low power and RF devices, covering specific module development for 130, 90 and 65 nm PD SOI. Electrostatic discharge (ESD) device studies were done in PD SOI 130 and 65 nm; and
3. SOI materials developments, including SOI and high resistivity substrates for RF applications, and ultra thin film SOI for FD SOI for ultra low power applications in 200 and 300 mm wafers.

Results demonstrated the interest of high resistivity SOI substrates for digital and RF

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applications. In 130 nm demonstration devices and circuits, comparing PD SOI with bulk achieved:

- 10 to 20% increases in speed of SRAM memory and standard cells, depending on device area;
- Dynamic power requirements up to 40% less;
- Up to 40% increased inductance Q factors as there are no eddy currents in the high resistivity substrate;
- Smaller insertion loss for RF as substrate resistivity is much higher; and
- Decreased crosstalk through the high resistivity substrate between logic and analogue or RF blocks compared with standard resistivity SOI or bulk wafer substrates.

  In addition, the high resistivity decreases line losses in on-chip transmission lines.

Niche market previously

Until now, higher materials and processing costs have restricted SOI at an industrial level to niche markets where switching speed and/or power were critical. SOI was developed by IBM initially for high performance applications in computers, and IBM has licensed its SOI technology in the USA for the fabrication of high performance central processing units (CPUs) for laptop and personal computers. AMD is also producing performance CPU chips on 300 mm PD SOI wafers for laptop and personal computers.

However, new designs for lower-power handheld computing, communications and multimedia devices are now seen as potential future volume applications for SOI. And other markets, such as diagnostics and controls for combustion engines, could well benefit from the ability of SOI devices to operate at high temperatures.

The MEDEA+ consortium targeted very low power, efficient RF applications for mobile communications terminals. The project has already resulted in a commercial product: STMicroelectronics had an antenna switch by the end of 2006 based on SOI technology.

And the hunt is on for new customers. As an example, GSM mobile phones use CMOS or BiCMOS for front-end and baseband sections. Customers are now interested in SOI for the RF part to improve efficiency and its use is being evaluated for new multiband systems. The 130 nm products demonstrated in the MEDEA+ project are possibly too late for purely digital logic but this approach is now being studied for 65 nm low power SOI, with discussions going on with market leaders in the GSM and mobile terminal market.

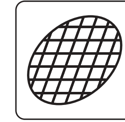
Of the three chipmaking partners, STMicroelectronics is already developing a range of SOI components for communications, Freescale is interested more in high performance applications, but NXP is biding its time as it is more oriented to consumer electronics, where this technology is not yet needed.

On the materials side, wafer manufacturer partner SOITEC has developed good business with its SOI wafers. Its 200 mm wafers are already on the market and 300 mm wafers are available, both with standard and high resistivity substrates.

Set for future

For CMOS, the trend is to the 45 or 32 nm nodes with the need for very shallow junctions and shorter channel lengths. SOI could well be the solution as the thin films involved in SOI are ideal for thin junctions and make better control possible.

The outlook for SOI is therefore particularly interesting. STMicroelectronics and its Crolles 2 Alliance partners already have a contract to evaluate future 32 nm SOI technology. And further research projects will probably be more applications oriented.



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KEY PROJECT DATES:

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MEDEA+ Σ!2365 is the industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.