PROJECT RESULT

Design methodologies

A502: Multi-processor embedded systems architecture (MESA)

# Efficient design methods boost computational power

**With IC geometries shrinking to 90 nm and below, multi-processor system-on-chip devices allow dramatic increases in computational power for mobile communications, consumer multimedia appliances and data-processing systems. The huge market potential makes development of efficient design methods a high priority for chipmakers and customers. In MESA, top European players joined forces to meet this need by targeting reconfigurable multi-processor architectures. Their flexible approach produced breakthroughs available to IC designers in several market segments and resulted in three spin-off companies.**

In addition to existing constraints inherent to designing mixed analogue-digital system-on-chip (SoC) devices, the transition to parallel processing presents chipmakers with new challenges. Factors such as scheduling, process communication, resource management and verification in the complex environment all need to be addressed.

Tackling such problems required advances in several key areas:

- New approaches for interface synthesis;
- In-depth analysis of software code for the specification and synthesis of a specific operating system, plus development of the sophisticated code-generation techniques needed to produce it;
- Improvement of inter-processor communication, via either circuit switching — including reconfigurable computing — or packet switching; and
- Use of formal verification as an alternative to classical methods for system validation — an area in which a huge amount of work had hitherto produced only limited results.

## Successful formula

A core team of five European industry leaders formed a consortium comprising developers, hardware and software suppliers, and users — large enough to give critical mass to the ambitious MEDEA+ A502 MESA project.

Coordinated by chipmaker STMicroelectronics, the industrial participants represented a rich variety of application areas, including telecommunications terminals (Alcatel), digital radio communication networks (EADS Telecom), consumer appliances (Philips) and computers (Bull). They were joined by six prominent research institutes and ten specialist computer-aided design (CAD) software vendors.

Many of the partners had co-operated in the earlier MEDEA SMT project, which focused mainly on single-processor architectures. That project resulted in the creation of four European start-ups, more than 110 new jobs in small European CAD companies, and 18 new CAD tools.

The same successful approach was followed in the MEDEA+ project to meet the challenges posed by multi-processor systems. MESA's five industrial partners agreed a common design flow, starting from application analysis. The purpose of this flow was to improve both the design approach, with higher flexibility and fewer design iterations, and the resulting SoC devices — more complexity, higher computational power and lower consumption. This proved to be particularly fruitful, leading to solutions for partitioning, simulating and linking the various processes needing to be executed in parallel. These included: architecture exploration focusing on communication nodes, task concurrency

management, co-simulation of heterogeneous multi-processor architectures, communications architectures and optimisation of parallelism with respect to speed or density.

## Early decisions

MESA's proposed methodology allows design decisions to be taken at a very early stage and at a high level of abstraction, which will help in handling densities around 400 million transistors/cm$^2$ possible with emerging 65 nm technology.

By the end of MESA, application-specific integrated design platforms had been defined for software radio and audio devices, as well as generic platforms for wired and wireless telecommunications, on-chip communication, processor/code development and verification. The results will facilitate the transition to parallel processing in terms of both design — through reduced design time, design size optimisation and accuracy — and circuit operation by higher execution speed, lower power demand and reduced silicon area.

New methods allowed automation of actions such as code optimisation, previously performed manually, as well as others such as power estimation, which formerly occurred later in the design flow. Some already automated actions were also significantly accelerated — in the case of simulation by between one and four orders of magnitude. Although, by definition, design entry will always be manual, here too the time required was halved. Another outcome was that blocks larger than half a million gates can be handled by formal verification.

A more efficient use of hardware resources permitted the realisation of smaller memory footprints and faster processor execution, with fewer cycles and reduced risk of deadlocks. To address the burgeoning market for portable applications, new analysis and optimisation techniques were proposed to reduce power consumption.

## Application-oriented results

The MESA project proved that MP3 audio decoding becomes affordable at power levels below 1 mW. The risk of hardware malfunction is reduced by adaptation of formal verification to mainstream design flow, while software problems are minimised by early bug detection. The project reviews were illustrated by seven live demonstrators showing complex stream-based applications — from 3D graphics and an MPEG4 video decoder, to software radio, voice and face recognition, and a hearing implant.

High-level design flow standards were aligned between the industrial companies, which will simplify interoperability and the exchange of models. Moreover, the support of top European enterprises will encourage more widespread adoption of these standards.

In all, following the end of the project, in-house exploitation of 22 tools and methods has begun while nine European CAD companies are ready to begin commercial marketing of 13 products. These CAD firms include three start-ups resulting from the project itself.

Further projects have been launched or are planned to build on the achievements of this MEDEA+ project. One will continue the research into inter-block communications, seeking to replace the traditional bus structure with entirely new concepts.

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**PARTNERS:**

ACE
Alcatel-Bell
ARM (former Adelante)
Bull
CAPS-Entreprise
CoWare
EADS Telecom (former EDSN)
IMEC
INRIA
Metasymbiose
Philips
Polyspace
STMicroelectronics
TCT
Uni Grenoble/TIMA
Uni Leuven (KUL)
Uni Nantes
Uni Paris/LIP6

**PROJECT LEADER:**

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**KEY PROJECT DATES:**

Start: January 2001
End: December 2004

**COUNTRIES INVOLVED:**

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Italy
The Netherlands

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