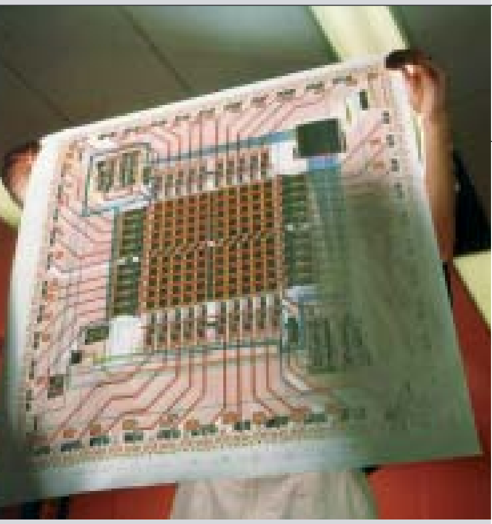
PROJECT RESULT

Design methodologies



A510: Analog enhancements for a system to silicon automated design (ANASTASIA+)

Fixing the formula for mixed-signal chip design

Design automation for analogue and mixed analogue-digital-signal circuits and systems is still lagging behind that which has been achieved in the digital area and, if anything, the gap is widening as circuit complexity grows. In the MEDEA+ A510 ANASTASIA+ project, a combination of top-down and bottom-up approaches has achieved substantial progress towards the realisation of a seamless process for system-to transistor-level design. Accurate mathematical analysis can now replace methods involving approximation followed by time-consuming trial and error for the definition of key parameters.

There is increasing demand for application-specific integrated circuits (ASICs), with growth forecast to increase annually by more than 30%. Europe is the leading developer and manufacturer of such mixed-signal devices, with a market share of over 40% and strengths in the automotive and telecommunications sectors. A continuing ability to reduce development costs and shorten time to market is thus key to the competitiveness of European chipmakers, system houses and computer-aided design (CAD) suppliers.

As technology permits ever-higher levels of circuit integration, systems can be built from far fewer components. The side airbag actuator of a modern car, for example, consists only of a sensor, an actuator and a single controller chip. Consequently, individual devices increasingly determine the behaviour of entire systems.

Since most system-on-chip (SoC) designs include analogue components, the lack of a fully automated design process for these elements creates a serious bottleneck in the path towards cost-effective production.

Targeting seamless design

The MEDEA+ A510 ANASTASIA+ project set out to develop seamless top-down design methods for integrated analogue and mixed-signal systems (A/MS), and to achieve a high level of automation and reuse. However, simultaneous design of digital and analogue system components required significant extensions to available methods and tools. The very advanced methods used in digital design – system partitioning, logic synthesis and layout synthesis – had to be combined with the topology selection, sizing and layout methods used in analogue design for an efficient and effective overall methodology. Specialised electronic design automation (EDA) tools were already available for many individual stages, but no satisfactory solutions existed for performing the step from one level to the next, or for system simulations with mixed abstraction levels.

An ideal solution would have been to pursue a purely top-down approach, with numerical simulation extending from total system specification, through block modelling, to layout. Unfortunately, rapidly advancing technology makes this impractical, as resulting second order effects cannot be accommodated in the top-down algorithms. So, it was necessary to combine top-down design and refinement with bottom-up validation methodologies.

To tackle these issues, a consortium including system and chip manufacturers, universities, research institutes and CAD specialists was assembled under the coordination of Infineon Technologies. While participants were able to draw on results of the earlier MEDEA ANASTASIA and SADE projects, their work covered a much wider horizon. This was made possible by the involvement of tool providers such as Mentor Graphics, new start-up MunEDA and Fraunhofer ITWM, as well as a broader set of application partners. Moreover, they could profit from the fact that A/MS languages had matured into well-defined standards providing a framework for the whole design cycle.

Progress was aided by collaboration with other MEDEA+ consortia, and with the German national Ekompass programme.

World-leading developments

ANASTASIA+ led to development of several new-generation tools to a prototype or commercially exploitable stage. A major breakthrough was application of enhanced symbolic analysis to CAD knowledge acquisition to dramatically reduce analysis time and speed failure detection for analogue blocks at transistor level. Such analytical methods have also been developed for non-linear circuits, allowing semi-automated generation of behavioural models. In addition, there has been significant progress in modelling of analogue blocks for devices such as analogue-digital converters.

To increase reuse of behavioural models, a tool was developed that automatically generates documentation from the model source code and tagged comments. Furthermore, a library concept was defined that eases use of the behavioural models. Both are prerequisites to enable simulation of bigger analogue and mixed-signal blocks.

Behavioural modelling is key to modern circuit design. Before, models were manually coded: a time-consuming and error-prone task. New simplification methods have been developed and implemented in the Analog Insydes toolbox from Fraunhofer. This accelerates circuit analysis and failure detection by at least two orders of magnitude, with a guaranteed accuracy of the derived formulas.

Another highlight was a new method of design centring for yield optimisation. Here too, the time and cost of worst-case calculations using conventional simulations was proving unreasonably high with today's design complexities. The WiCkeD (Worst-Case-Distances) tool — now commercialised by MunEDA — offers a unique combination of analytical features and algorithms for this purpose.

The strength of the consortium also enabled the partners to exert considerable influence on the international standardisation bodies. This was particularly notable with regard to the extension of the SystemC language to include mixed-signal components, leading to the founding of a special working group.

Continuing need

As well as enabling the manufacturing partners to reduce development times for new products, ANASTASIA+ will benefit European industry in general through the commercial availability of Analog Insydes and WiCkeD, plus the distribution of the newly generated design methods via networks of SMEs. At the same time, the project has identified new problems, notably in the areas of design for manufacture and design for yield, that will need to be addressed in follow-up research.

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PARTNERS:

Analog Microelectronics (until 2002)
Atmel
CISC Semiconductor Design and Consulting (from 2002)
EADS Telecom
FhG-ITWM
Infineon Technologies
IMMS (from 2003)
Melexis
Mentor Graphics
MunEDA (from 2003)
Philips (from 2002)
Robert Bosch
Sci-worx
Siemens MC

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End: December 2004

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Italy
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