PROJECT RESULT

Design Methodologies

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A5II: Tools and methods for IP (ToolIP)

IP reuse methodology speeds time to market

The functionality of today's electronic devices – from laptop computers and mobile phones to domestic multimedia and automotive equipment – depends increasingly on complete system-on-chip devices. The challenge is to make the design cycle for these systems ever shorter to improve market position and meet customer expectations. One way to reduce the time-to-market for such devices is to reuse as much as possible of existing designs. The MEDEA+ ToolIP project has developed a set of tools that can facilitate intellectual property reuse and validation, and help to ensure first-time silicon success.

Reuse of integrated circuit designs is essential to speed development of system-on-chip (SoC) devices. However, design engineers need to be aware that suitable intellectual property (IP) exists, and it must be both in a format that can be incorporated painlessly into the design in progress, and that it will interface and function correctly with other parts of the design.

The MEDEA+ A511 ToolIP project set out to develop tools and promote standards that make IP reuse more attractive. In some areas, this requires design engineers to rethink the way they work. ToolIP considered IP in terms of its qualification, a term that embraces IP selection, evaluation, modification, validation and simulation. This did not require new languages or large investment in capital and time. ToolIP methodology provides the missing element in the existing SoC design chain. This will maximise the reuse of existing IP and help to guide system architects to finding appropriate IP in a timely manner.

Time-consuming process

ToolIP involved a well-balanced consortium made up of major European semiconductor and system companies, IP providers and reuse infrastructure vendors. An important consideration was that the selection process for each IP user was complex and time-consuming. No tools were available for the location, selection and evaluation of potential IP, making the whole process somewhat difficult. The challenge therefore lay in defining a complete IP specification methodology.

Previously, existing IP was often not even considered during the specification phase of a new product because of inadequate parameterisation or insufficient executable specifications with simulation and system behaviour characteristics. Even with an adequate specification methodology, existing structures for searching and locating for IP provided only static navigation or simple text-based syntactic searches, which ultimately resulted in the IP not being reused.

Mechanisms were needed therefore to locate the most appropriate IP – necessitating a search in terms of acceptable quality criteria that included compliance, testability, adherence to standards, performance, area, power and timing issues. The system architect also wants assurance that the IP has adequate documentation, portability and maintainability.

The MEDEA+ project addressed the complexity of current system design in networking, high-speed links, multimedia and automotive domains using system-level modelling and verification techniques,

applying design reuse with qualified and parametric IP cores, and providing a seamless design flow integrating existing and emerging tools. The resulting IP-based system level modelling and simulation design methodology in particular represents a breakthrough in current design methodology, which would lead to a strong impact on competitiveness and standardisation.

Sharing IP directly

In practical terms, consortium partners such as chipmakers STMicroelectronics and Philips each had their own way of doing things. They had their own guidelines for handling IP, which clearly stated the methodology to be used in providing IP for reuse. Now, with the methodology developed by ToolIP, they can all use similar procedures for verifying and validating their respective IP, and this will enable them to share IP more easily. This applies equally to the systems and IP providers involved in the MEDEA+ project – and the results are also being disseminated through the research institutes and universities. This is leading to more mature and more flexible IP exchange practices.

The MEDEA+ project came together in the first place at the suggestion of design engineers. Work was already in progress separately for handling both low-level – register-transfer level (RTL) and below – and high-level transaction-level modelling (TLM) model IP reuse. It made good sense to combine these two activities and benefit from the wider consensus that a large project could deliver.

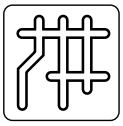
ToolIP has also been active in the standardisation arena. It is involved with the Virtual Socket Interface Alliance (VSIA) for the characterisation of IP reuse and interfaces. It is also involved in the Open SystemC Initiative (OSCI) – the industry organisation backing SystemC as an open-source system-level chip design language – for the language working group. One of the main achievements was the SystemC 2.0 language for IP specification and reuse.

Reducing marketing risk

The tools and methodology developed by ToolIP will enable Europe to maintain its competitive edge in a fast moving global market. Electronic products that incorporate SoC built by reusing IP can be brought to market more quickly.

An important side effect is that the MEDEA+ project will enable small and medium sized enterprises (SMEs) to participate in systems development, for example by developing reusable IP or systems that incorporate reusable IP. Since the IP blocks will have been verified and validated, the overall development time is reduced and the so-called 'marketing windows of opportunity' will not be missed.

Results of this MEDEA+ project will continue to be shared through technical articles, conference papers and the organisation of workshops. Some 80 articles have already been published. IP quality criteria standardisation in the VSIA framework will also support exploitation by increasing demand for qualified IP.



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Partners

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Empolis Knowledge Management
FZI Karlsruhe
IMSE-CNM
Infineon Technologies
ISD
KORG Italy
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SIDSA
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Thales Communications
Thomson
TILAB
Tima
Uni Ancona
Uni Bologna
Uni Madrid
Uni Paderborn

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Key project dates

Start: January 2001
End: December 2003

Countries involved

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Germany
Greece
Italy
The Netherlands
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