PROJECT RESULT

Process equipment

T302: Atomic layer deposition for 100nm devices (ALADIN+)

Atomic monolayers help push chip limits

Markets for personal electronic devices such as mobile phones and palmtop computers have grown markedly as they become smaller, lighter and more sophisticated.
Much of this is thanks to chip manufacturers, who have been able to reduce gate size and so fit more functionality on the chip. But there is a limit to how far this shrinkage process can be taken. These limits have been successfully challenged by the MEDEA+ T302 ALAD1N+ project, which has developed a viable process that builds structures using atomic monolayers. The result will help improve Europe's position in global chip manufacture.

With existing semiconductor fabrication processes, there is a limit to how small the individual components can be shrunk. Linear dimensions can be reduced, but there comes a point where conventional dielectric materials, which are used for both insulating and retaining electrical charge, no longer work satisfactorily. Silicon dioxide (SiO_2) has been used as a dielectric for CMOS device fabrication for 30 years now, and its properties are well known. For device technologies of less than 100 nm, however, the leakage current through SiO_2 layers is too high and an alternative material is required.

The insulating property is important because it limits both the thickness of successive layers and the rate at which electrical charge leaks away. Layers could be made thicker to counteract leakage, but then the capacitance, which stores the charge, is reduced. Using a so-called 'high-k' material such as hafnium oxide, with higher dielectric constant than SiO_2, is the only way to increase capacitance.

Sequential layer deposition

The process developed by the MEDEA+ T302 ALAD1N+ project is known as atomic layer chemical vapour deposition, or ALD for short. In conventional semiconductor fabrication, chemical reactants are mixed together and react either on the wafer's surface or in the gaseous phase. In the ALD process, the reactants are applied separately but sequentially in the form of thin films. The first reactant is applied to the semiconductor wafer and is adsorbed by the surface, then the excess is washed away leaving an atomic monolayer. The second reactant is then applied, reacting with first layer, and so on. The process continues, producing A-B-A-B layers until the desired thickness is achieved.

A typical dielectric layer of high-k hafnium oxide is between 2 and 4 nm thick. Each atomic monolayer is around 0.2 nm thick, so the dielectric feature is typically ten layers deep. Each cycle of the process lasts only a few seconds, so the dielectric layer can be built up in a matter of minutes. The number of atomic monolayers deposited determines the overall thickness precisely.

The ALD process brings about a dramatic improvement in leakage current – by a factor of between 10^4 and 10^6. This will enable integrated device manufacturers to make semiconductor chips with lower standby power. For the consumer, this translates to smaller mobile phones and lighter laptop computers.

The project focused on two main areas. The first was the development of integrated processes and equipment for making gate dielectrics and gate electrodes. The second area was the development of integrated processes and equipment for barrier and seed layer deposition in dual damascene (inlaid) structures.

Within this second area, for example, ALAD1N+ developed a process for making very thin barrier layers prior to metallisation. This was necessary to shrink the size of the interconnections that link the various devices together. Such an approach was an essential factor, together with the small device size, to increase overall packing density.

Teamwork behind success

The ALAD1N+ consortium comprised equipment, semiconductor, consumer equipment and research companies in Belgium, Finland, France, Italy and the Netherlands. The project is co-ordinated by major wafer-fabrication equipment manufacturer ASM, a world leader in ALD technology. The consortium came together just as the problem of high-k dielectrics was becoming apparent. It was realised that this was going to be a major problem, and that a concerted large-scale effort would be needed to tackle it.

It is unlikely that any one of the consortium members would have had the resources to carry out the necessary research and development on its own. Working as a consortium, unusually high value-for-money leverage has been achieved. What is even more remarkable is that the results have been achieved in the space of only two and a half years.

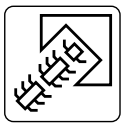
The consortium found working within the framework of MEDEA+ to be highly beneficial, with just the right balance between protecting the interests of individual consortium members and facilitating a useful information exchange. Furthermore, there was direct support for the project from the public authorities in Belgium, Finland and France.

Important factors for success were the regular reviews that are part of the MEDEA+ monitoring process. Much energy was put into these meetings, and a lot more happened than merely reporting progress to date. The meetings were well attended, usually with several representatives from each member of the consortium. All members contributed enthusiastically and automatically picked up their respective challenges without having to be bound into particular roles. A great deal of synergy took place.

From research to production

The project has achieved all of its objectives. The technology, on existing 90 nm fabrication facilities successfully tested in a trial system, will be applied in an operational system for the 65 nm chips coming off the production line in volume in 2005. In the meantime, new ALD fabrication equipment has to be designed, manufactured and installed, and the additional process steps incorporated into existing process flows.

Until now, it is the USA that has dominated the global chip-fabrication sector. The ALD process now puts Europe clearly in front in terms of the production of low-power devices. It will bring benefits and employment throughout the value chain, for manufactures of fabrication equipment right through to the end user.



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Partners

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Key project dates

Start: January 2000
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