CATRENE

Programme Review Report 8 - 2013

Full year report January-December 2013

EUREKA Σ! 4140

CATRENE

Cluster for Application and Technology Research in Europe on NanoElectronics

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Executive Summary

2013 has been an edifying year for CATRENE with a number of very informative and constructive inputs pointing to areas where the programme was strong and areas where it necessitated improvement.

The most complete input came from the mid-term assessment of the CATRENE Programme, which was launched in October 2012 by Public Authorities. The objectives of the assessment were to look back on the results achieved so far (economic and societal impact, outstanding research results and breakthrough) and to look forward on opportunities to shape a future EUREKA instrument for micro- and nanoelectronics.

The final assessment report and recommendations, delivered in April 2013, provided the tools necessary to move forward.

A Joint Working Group with participants from Industry and from Public Authorities was mandated to implement the recommendations as soon as possible and identify the long-term prospects for a new Eureka Cluster beyond 2015 adapted to meet new societal/industrial challenges in a changing global landscape. Its objectives: openness, simplification, cohesion and valorisation.

The following report will cover the progress and actions undertaken throughout 2013 in CATRENE to meet its primary objective, which is to foster technological Leadership for a competitive European ICT industry and to meet the objectives of the Joint Working Group as stated above.

Chapter 1 provides an overview of the CATRENE programme while chapter 2 and 3 focus more specifically on 2013 projects and actions.

- **Green light for continuation of CATRENE until end of 2015 and to begin working on beyond 2015**

The final assessment report was handed over to the CATRENE Public Authorities (CAPA, CATRENE Directors Committee) as well as to the CATRENE Board and Support Group. It was discussed during a common meeting between the CDC and the CATRENE Board in Stockholm on April 26, 2013.

The CATRENE Board and CDC both accepted the Assessment Report without amendment and recognised the excellent work undertaken by the assessment team.

The CDC concluded by giving a "GO" to the extension of CATRENE until end of 2015 with the obligation to analyse the report and to identify recommendations that could be implemented in the short-term, starting in 2014, in order to improve the running programme. The Committee also requested that reflections on long-term prospects for the future of CATRENE beyond 2015 start immediately in parallel.

- **Overview of CATRENE**

The CATRENE programme opened its 1st Call for Project Proposals on 29 February 2008. Today, a total of 6 calls have been launched resulting in 58 labelled projects and a total effort of more than 8400 PYs.

As of 2S 2013, 14 CATRENE projects have successfully ended.

- **Results of CATRENE Call 6**

In 2013, CATRENE launched its 6th Call for Project Proposals. Altogether, 9 projects were labelled amounting to 1296 PYs.

For the first time, through Call 6 projects, partners from Canada and South Korea will be participating in the programme.

Also of interest is the project E450LMDAP, which is the first project to receive a label from both the ENIAC Joint Undertaking and CATRENE.

- **European Nanoelectronics Forum 2013**

The sixth edition of the European Nanoelectronics Forum took place in Barcelona, Spain on 27-28 November 2013 under the theme *Innovation for Growth*.

Jointly organized by the EUREKA Cluster CATRENE, the ENIAC Joint Undertaking and the European Commission, the event had a record participation with 345 attendees from all over Europe.

During the forum, the project PANAMA received the CATRENE Innovation Award for its outstanding work in a number of key communications application areas and allied technologies.

The feedback received in the questionnaire sent to participants at the end of the event showed a high level of satisfaction and gave ideas that will be implemented in 2014.

Under the guidance of the Joint Working Group, the objectives for the CATRENE Programme in 2014 will be to execute the 7th Call for Project Proposals as well as to put into action the recommendations of final assessment report, in order to improve the existing programme and prepare for a new Cluster on Nanoelectronics for beyond 2015.

1

Overview of CATRENE

1. Overview of CATRENE

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				Out of the labelled are:			
Call	PO received	FP received	Labelled	Cancelled /merged/ transferred/ suspended	Successfully Ended	Active	Out of active are in start-up phase
1st Call	**17**	**14**	**14**	**5**	**8**	**1**	**0**
Applications	10	8	8	3	4	1	0
Technologies	7	6	6	2	4	0	0
2nd Call	**14**	**10**	**10**	**3**	**6**	**1**	**0**
Applications	9	7	7	3	3	1	0
Technologies	5	3	3	0	3	0	0
3rd Call	**15**	**10**	**10**	**3**	**0**	**7**	**0**
Applications	7	4	4	2		2	0
Technologies	8	6	6	1		5	0
4th Call	**19**	**14**	**10**	**1**	**0**	**9**	**0**
Applications	10	8	7	1		6	0
Technologies	9	6	3	0		3	0
5th Call	**8**	**5**	**5**	**1**	**0**	**4**	**0**
Applications	**5**	**3**	**3**	**0**		**3**	**0**
Technologies	**3**	**2**	**2**	**1**		**1**	**0**
6th Call	**13**	**10**	**9**	**0**	**0**	**9**	**9**
Applications	**9**	**7**	**6**	**0**		**6**	**6**
Technologies	**4**	**3**	**3**	**0**		**3**	**3**
Per 2S 2013	**86**	**63**	**58**	**13**	**14**	**31**	**9**

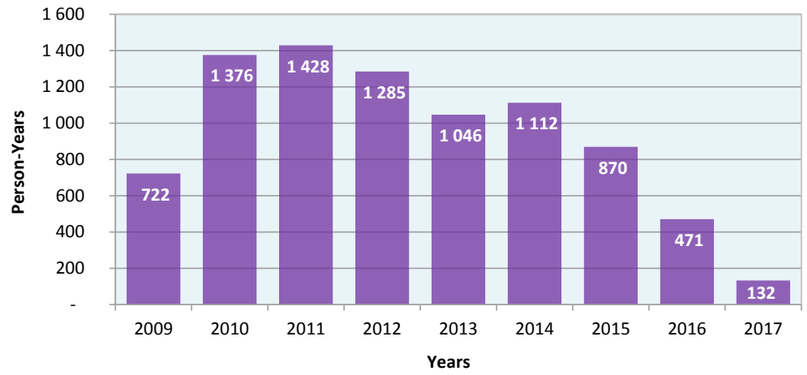
Over the course of the entire CATRENE programme, 13 projects were cancelled/merged due to national eligibility criteria, funding constraints and in some countries even as a result of reduced funding volume. In 2013, one project from Technologies labelled during the 5th Call was cancelled due to its re-allocation to another funding programme.

With the continuation of CATRENE programme until end of 2015, further calls for submission of project proposals are planned in the years to come.

Resources, participants and work areas

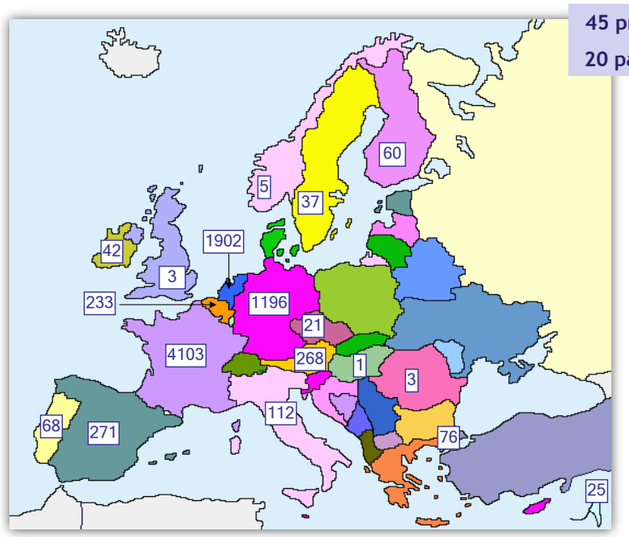
The following graphs provide an overview of the CATRENE project resources (in PYs), of their participants and of their related work area.

CATRENE Calls 1 to 6 labelled resources
Total PYs: 8 436*



*This figure does not include the person years of MEDEA+ projects which continued running until 2010.

CATRENE resources per country as per year end 2013



45 projects, 364 partners
20 participating countries

Total for 2009-2016:
8 436 PYs

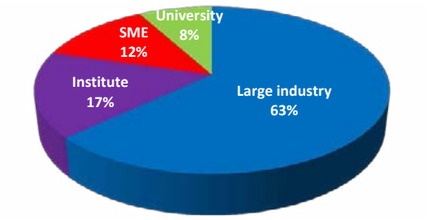
AUT:	268
BEL:	233
CZE:	21
DEU:	1196
ESP:	271
FIN:	60
FRA:	4103
GBR	3
HUN:	1
IRL:	42
ITA:	112
NLD:	1902
NOR:	5
PRT:	68
ROU:	3
SWE:	37
TUR:	76

Non-European countries

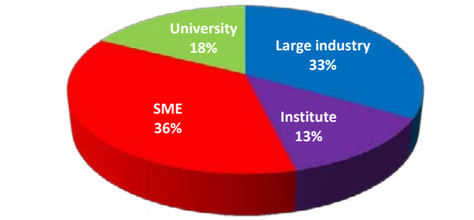
CAN:	3
ISR:	25
KOR:	9

Structure of CATRENE projects

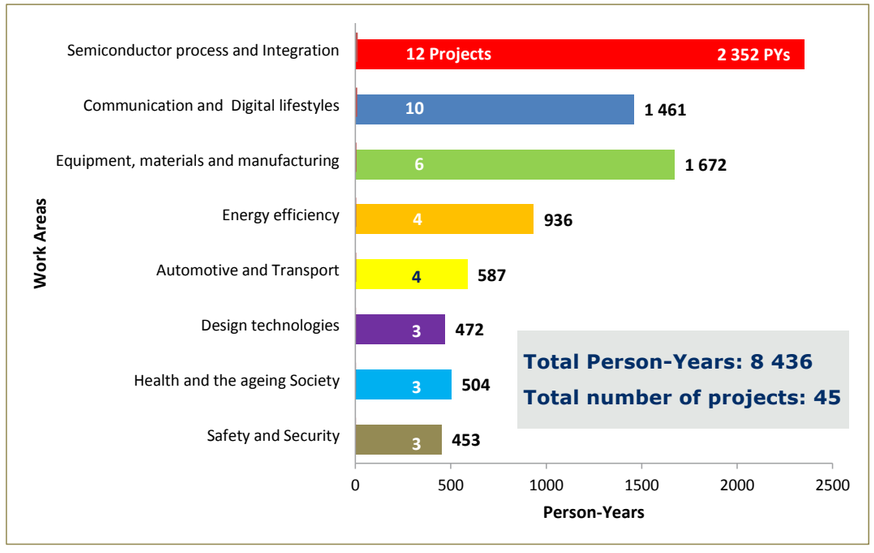
Total Resources: 8 436 PYs



364 participants from 20 countries



CATRENE labelled projects - split by work area



For a more detailed list of projects according to work areas, see Appendix B. CATRENE Projects Focus Matrix at the end of this document.

CATRENE
Programme Review - Year 2013

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2013 CATRENE Year in Review

2. 2013 CATRENE Year in Review

2.1 Achievements

2.1.1. Green light for continuation of CATRENE until end of 2015 and to begin working on beyond 2015. Creation of Joint Working Group between members of European R&D&I community and Public Authorities.

The mid-term assessment of the CATRENE Programme was launched in October 2012 by Public Authorities, driven by France, Germany and the Netherlands with the support of other involved countries. The objectives of the assessment were to look back on the results achieved so far (economic and societal impact, outstanding research results and breakthrough) and to look forward on opportunities to shape a future EUREKA instrument for micro and nanoelectronics.

The final assessment report was handed over and discussed in a common meeting between National Authorities and Industry in Stockholm on 26 April 2013. The report was approved by Public Authorities without amendment. All parties valued the excellent work undertaken by the assessment team.

The recommendations made in the final assessment report provided the tools needed in order to move forward. They point to areas where the CATRENE programme is strong and areas where it needs to be improved.

In view of the "GO" given by Public Authorities for the continuation of CATRENE until end of 2015 and to begin working on beyond 2015, a Joint Working Group was mandated to address the recommendations that could be implemented in the short-term and to begin, immediately, identifying the long-term prospects for a new Eureka Cluster beyond 2015 adapted to meet new societal/ industrial challenges in a changing global landscape.

The Joint Working Group, involving members of the European Nanoelectronics R&D&I community and National Authorities, has since worked together on the following processes and actions:

- an online questionnaire concerning CATRENE was launched and open to all to answer between June and July 2013. More than 160 responses were received from participants in 12 different countries. The questionnaire provided further detail to the assessment report and showed the strong support of the CATRENE programme by the respondents. The results also provided constructive ideas for the improvement of the programme;
- the reorganisation of the CATRENE Office was completed and resulted in the adoption of a rotating chairmanship between members of the Board and the merge of the Office Director function with the Technologies Director function (effective beginning of 2014);
- the improvement of overall communication, with the objective to become more visible, and provide increased clarity on the results achieved through CATRENE collaborative research projects;
- revalorisation of the CATRENE label, in order to increase the correlation between receiving a label and receiving funding;

- improved cohesion between Industry and Public Authorities,
- eliminate the closed-club perception of CATRENE, by increasing the information flow through new and improved communication tools such as a newsletter and a renovated website as well as the publication of a clearer call process.

Work is now on-going to further prepare for beyond 2015.

2.1.2. Call 6

In 2013, CATRENE launched its 6th Call for Project Proposals. The call opened with a Brokerage Event on 23-24 January in Paris, attended by more than 200 people from across Europe. During the event, some 28 project ideas for CATRENE and the ENIAC JU were identified and elaborated on.

CATRENE 6th CALL 2013

Call opens	**04 February**	Labelling sessions	**24 October & 18 December**
PO submission	**02 April**		
FP submission starts	**30 May**	Projects start	**01 January 2014**
FP submission ends	**12 September**		

Participation in Project Outline (PO) phase is mandatory for participation in subsequent Full Proposal (FP).

Altogether, 9 projects were labelled by CATRENE as a result of CALL 6 amounting to 1296 PYs.

It is important to note that, for the first time, partners from Canada and South Korea will be participating in the programme in the SMART-FE project labelled in Call 6. The project will be the first in the history of the CATRENE programme to have partners from outside of the Europe.

Also of interest is the project E450LMDAP, which is the first project to receive a label from both the ENIAC Joint Undertaking and CATRENE.

More details on the projects labelled in Call 6 are available in Chapter 3 of this publication.

2.1.3. Increased links and cooperation with other Clusters/Programmes

The mission of CATRENE is to promote and to strengthen the European nanoelectronics R&D&I community. CATRENE and other EUREKA Clusters have been recognised as the only initiatives directly managed by R&D&I actors in regular contact with the EUREKA network and Public Authorities.

According to its mission, CATRENE is cooperating with other initiatives and organisations supporting the nanoelectronics domain:

- CATRENE and its predecessor programmes exists since 1987 and has continuously collaborated with the other EUREKA Clusters.

- CATRENE has a co-labelled project with another EUREKA Cluster.
- An Inter-Cluster Committee has been created in 2010 to reinforce this cooperation.
- CATRENE has a strong link with the industry association “AENEAS” representing R&D&I actors in the ENIAC JU.
- CATRENE and AENEAS work together to define a common ‘Vision, Mission and Strategy’ (VMS) - the reference document for projects in CATRENE and ENIAC.
- CATRENE and AENEAS host a Common Brokerage Event each year to prepare upcoming CATRENE and ENIAC calls.
- CATRENE organises the annual European Nanoelectronics Forum with the contribution of the ENIAC JU and the European Commission’s FP7 where projects and speakers from the three programmes are presented.

2.2. Events

A number of events underlined the CATRENE communication strategy in 2013, reaching from the very technically oriented and network focused Brokerage Event for experts to the yearly European Nanoelectronics Forum, which has achieved a high level of recognition in Europe today.

2.2.1. European Nanoelectronics Forum 2013 and CATRENE Innovation Award

The sixth edition of the **European Nanoelectronics Forum** took place in Barcelona, Spain, on 27-28 November 2013. 345 participants from all over Europe attended the event organized under the theme *Innovation for Growth*. During the plenary session, the audience showed high appreciation for the speeches delivered, notably by Khalil Rouhana (European Commission), Kurt Sievers (NXP) and by 3 European RTOs together including Hubert Lakner (Fraunhofer), Laurent Malier (CEA-Leti) and Luc Van den hove (Imec). The Poster and Demo session was organized in an area of 1000 m^2 and presented more than 70 projects from CATRENE, the ENIAC JU and the European Commission’s FP7. New additions to the event this year also included a fully functional Twitter account allowing the public and journalists to follow all developments related to the Forum, as well as Talk Workshops during which hot topics were presented in an informal setting. The feedback received in the questionnaire sent to participants at the end of the event showed a high level of satisfaction and gave ideas that will be implemented in 2014.

The event was jointly organised by the EUREKA Cluster CATRENE, the ENIAC Joint Undertaking and the European Commission.

During the event, the project PANAMA (Power Amplifiers and Antennas for Mobile Applications) was chosen **2013 winner of the CATRENE Innovation Award** for its outstanding work in a number of key communications application areas and allied technologies.

The assessment of communications versatility and power efficiency shows that the power amplifier is the key component in the communications chain that could help achieve these objectives. However, advances in amplifier technologies need to be considered in the overall context of the communications system to ensure comprehensive efficiency improvements, rather than simply transferring the problem elsewhere.

PANAMA set out to address these needs with the use of integrated systems, discrete systems and distributed systems (co-located with the aerial), and applied to a set of target applications, such as 3G/4G and millimetre-wave mobile communications handsets and transceiver base stations, avionics, mobile satellite communications and home networking. Not only did PANAMA meet the efficiency gains it set out, but all (power-efficiency) techniques and methods (pertaining to integrated and discrete systems dedicated to 2G/3G mobile applications, home networking, base stations, airborne and sitcom) that were developed or optimised surpassed their expected efficiency targets.

The CATRENE Innovation Award is bestowed each year to a project with a high level of innovation and far-reaching exploitation potential, market impact and overall benefits for Europe, as well as, creative objectives and effective management.

The next European Nanoelectronics Forum will be held on 26-27 November 2014 in Cannes, France.

2.2.2. Common AENEAS and CATRENE Brokerage Event 2013

The AENEAS and CATRENE Common Brokerage Event 2013 was held in Paris on 23-24 January. The objective of this networking event was to provide CATRENE partners and AENEAS members (participating in the ENIAC JU) with the opportunity to brainstorm about future projects and initiate consortia building.

The programme of the event was based on sessions covering the work areas common to both the CATRENE White Book and the ENIAC JU Multi-Annual Strategic Plan:

- Communication and Digital lifestyles
- Automotive and Transport
- Energy Efficiency
- Safety and Security
- Health and the Ageing Society
- Design Technologies
- Equipment, Materials and Manufacturing
- Semiconductor Process and Integration

During each session, a designated leader moderated the discussion around new project ideas along with consortia building.

During the 2013 edition, 28 project ideas were identified and elaborated on.

AENEAS and CATRENE has organised this event together since 2009. With 135 participants in 2009 and over 200 participants in 2013, the event is now recognised as a key networking event for the

European nanoelectronics community and the first step in the elaboration of both CATRENE and/or ENIAC JU projects.

2.2.3. CATRENE Scientific Committee Workshop:

Power Devices Enabling Higher Energy Efficiency

See 2.3.1

2.2.4. CATRENE Design Technology Conference 2013

The **CATRENE Design Technology Conference** was held in Dresden, Germany on 14-16 May 2013 in conjunction with the edaWorkshop13 by edacentrum.

Together, the events provide a comprehensive overview of latest algorithms and tools, emerging technologies, key and partially common CATRENE and IKT 2020 projects, as well as advanced research in application oriented SoC design automation in Europe.

Attracting European experts from industry and academia, approximately 150 participants attended the event. The mix of representatives from industry and academic created ideal opportunities for a professional exchange of ideas on a scientific basis. The dialog paved the way for industry to benefit from research results. It promoted communication between EDA experts and public authorities, and supported the dissemination of the results of publicly-funded projects.

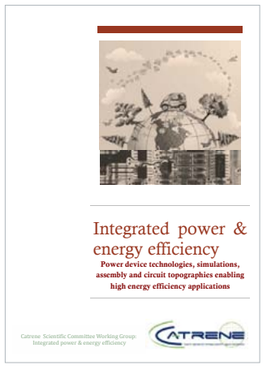
People involved in the projects were invited to present their results by means of talks and posters. At the heart of these presentations was the relevance of the applications to topics affecting society (as defined in IKT 2020 and CATRENE White Book, part B). As second essential part of the event, the project presentations were supplemented by a selection of peer-reviewed scientific papers on R&D results.

Held annually since 2009, the CATRENE DTC has become the meeting point for Europe's scientists and experts in applications-oriented design.

2.3. Publications

Several publications have been undertaken in 2013 by CATRENE bodies focusing, for example, on a domain of high importance for the European Nanoelectronics R&D&I community such as the Scientific Committee Report on Integrated Power and Energy Efficiency or on the revision of strategies per domain in the updated Part C of the Vision, Mission and Strategy document. A summary of each publication follows below.

2.3.1. Scientific Committee Report on Integrated Power and Energy Efficiency



The report, which received a high level of support from Industry, was officially presented in January 2013 in Paris during a workshop that gathered more than 60 participants.

The CATRENE Scientific Committee released the 'Integrated Power & Energy Efficiency' report in January 2013 during a workshop in Paris that gathered more than 60 participants. The report received a high level of support from Industry and is available for download on the CATRENE website.

The goal of this document is to provide the CATRENE community with a status on Integrated Power & Energy Efficiency and to propose orientations for future development in this domain in which the European industry is or can be a key player.

Highlighting the role of power electronics in improving energy efficiency, the document presents a summary of the main advances in device technology including Si, SiC and GaN-based active devices as well as new solutions for passive devices. Integration in systems of wide band gap devices, in particular GaN devices, is also treated in the document with specific attention paid to thermal management, EMC/EMI. Last, but not least, the necessity to develop specific simulation tools for this kind of devices is clearly pointed out.

2.3.2. EUREKA Cluster Document

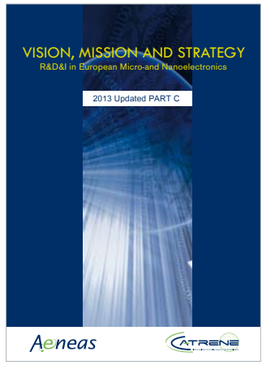
"Together, these EUREKA Clusters now represent 70% of the budget of the EUREKA portfolio and in total have leveraged some 14.9 billion euro in R&D efforts since EUREKA's inception."

Under the Turkish EUREKA Chairmanship (2012-2013), CATRENE has taken part in a HLG Working Group to produce a EUREKA Cluster Document. This report features five chapters that detail what EUREKA Clusters are, what makes them essential and the success of their impact on new economic and societal challenges.

The document serves to demonstrate to the public what a EUREKA Cluster regularly achieves through dynamic coopetition. The continuous growth and development of EUREKA Clusters, strongly supported by the European industry, EUREKA High Level Representatives and Public Authorities of participating countries, have made the Clusters what they are today: essential instruments for the global competitiveness of European industry.

The EUREKA Cluster document has become an important resource for all persons interested in learning more on cooperative R&D&I in Europe.

2.3.3. 2013 Updated Part C of the AENEAS and CATRENE VMS



An update of the Vision, Mission and Strategy document, common to both AENEAS and CATRENE, was undertaken in 2013.

The revision concerned only Part C of the document, which describes strategies per domain to a level that it can be used as reference for the creation of projects in ENIAC (to be succeeded from 2014 onwards by ECSEL) and CATRENE.

Compared to the previous part C of the VMS, the modifications being made aimed to: actualise the content (taking into account the strategic objectives of H2020; and extend the content in order to include lower (down to level 2) and higher (up to level 8) Technology Readiness Levels. This update is relevant for the Call 7 of CATRENE and first call of ECSEL. The updated part C will constitute the contribution by AENEAS to the MASP of the new ECSEL JTI.

AENEAS and CATRENE have, in the past, successfully achieved by this cooperation a strategic coordination of the EUREKA and ENIAC JU programmes in the field of nanoelectronics. With the help of all actors involved, their aim is to continue this coordination as much as possible through an alignment of the strategic objectives for Nanoelectronics R&D&I in Europe.

2.4. Press Coverage

The overview of 2013 press coverage is available on the CATRENE website in the communication section under Press Clips, and includes a link to view the complete text.

Article	*Source*	*Country*	*Date (Year 2013)*
CATRENE calls for proposals	Electronics Weekly	GBR	08 February
100 billion € for the European Nanoelectronics Industry	Microelectronic News	GBR	February
Nanoélectronique: 84 projets européens de R&D ont reçu 3 milliards d'euros en 5 ans	ElectroniqueS	FRA	February
EDAWorkshop 13 and CATRENE Design Technology Conferences (DTC)	Coventor	FRA	03 March
Flexible RFID-sensor tag could reduce global food waste	Holst Centre	NLD	14 March

Article	*Source*	*Country*	*Date (Year 2013)*
Communicating with Silicon	International Innovation	GBR	07 May
edaWorkshop13 and CATRENE DTC	Newsletter edacentrum 01 2013	DEU	May
CATRENE started Call 6	Newsletter edacentrum 01 2013	DEU	May
Europe in 10 billion € bid to boost chip industry	EETimes	GBR	23 May
Feu vert pour la poursuite du programme Eureka CATRENE jusqu'en 2015	VIPress.net	FRA	29 May
Microélectronique: feu vert des autorités publiques pour la poursuite du programme Catrene jusqu'en 2015	ElectroniqueS	FRA	05 June
CATRENE EXEPT A breakthrough in EUV technology	EUREKA News	BEL	16 September
Slimme sensoren tegen verlies in de voedselketen	Agentschap NL	NLD	08 November
Europäische Forschung und Entwicklung im Halbleiterbereich näher beleuchtet	Elektronik Praxis	DEU	18 November
An innovation based on sensors aims to fix the problem of food waste	EUREKA News	BEL	21 November
European Nanoelectronics Forum: Innovation for growth	EUREKA News	BEL	04 December
Le projet Panama récompensé par le Prix de l'innovation à l'European Nanoelectronics Forum	Télécom Bretagne	FRA	December

Article	Source	Country	Date (Year 2013)
Semi Europe organise le «European 3D TSV Summit 2014», un colloque sur les connexions traversantes qui se tiendra à Grenoble du 20 au 22 janvier prochain	ElectroniqueS	FRA	December
Industry News			
The 2013 Rocky Horror Semi Show	electronicsweekly	GBR	24 January
Introducing the new European strategy for micro- and nano-electronic components and systems announced – 23 of May 2013 – by Neelie Kroes during a press conference.	European Commission	BEL	23 May
Commission proposes New European Industrial Strategy for Electronics – better targeted support to mobilise €100 billion in new private investments	European Commission	BEL	23 May

CATRENE
Programme Review - Year 2013

3

Review of Call 6 & Projects Ended in 2013

3. Review of Call 6 and Projects Ended in 2013

Altogether, 9 projects were labelled by CATRENE as a result of Call 6 amounting to 1296 PYs.

It is important to note that, for the first time, partners from Canada and South Korea will be participating in the programme in the SMART-FE project labelled in Call 6. The project will be the first in the history of the CATRENE programme to have partners from outside of the Europe.

Also of interest is the Call 6 project E450LMDAP, which is the first project to receive a label from both the ENIAC Joint Undertaking and CATRENE.

Over the course of 2013, 6 CATRENE projects were completed successfully.

More information on the projects of Call 6 and on the projects ended in 2013 follows below.

3.1 Call 6 & unsolicited projects (labelled in 2013)

3.1.1 Overview Table

Call #	Project Number	Acronym	Work Area	Index
6	CT215	SMART-FE	Semiconductor process and Integration	3.1.2
6	CT217	RESIST	Semiconductor process and Integration	3.1.3
6	CT218	E450LMDAP	Semiconductor process and Integration	3.1.4
6	CA114	WiCon	Communication & Digital Lifestyles	3.1.5
6	CA116	CORTIF	Communication & Digital Lifestyles	3.1.6
6	CA118	FITNESS	Communication & Digital Lifestyles	3.1.7
6	CA208	MobiTrust	Safety and Security	2.1.8
6	CA405	INSIGHT	Health and the Ageing Society	3.1.9
6	CA507	GREETINGS16	Energy efficiency	3.1.10

3.1.2. Project CT215 SMART-FE

SOI + MEMS Advanced Reliable Technology for Front-End Module

Project leader: Jean-Louis Carbonero (STMicroelectronics)

Brief description:

This project aims at the integration of tuneable duplexers and filters in a high resistivity substrate CMOS SOI process for 4G Front End Modules and will therefore reduce the size and cost of the Front-end module (FEM) in smartphones or tablets. As one single duplexer will replace multiple off-chip duplexers, it will reduce the Bill Of Materials (BOM) and complexity. A SOI silicon manufacturer and specialists of RFMEMS either for the process, modelling and design constitute the project consortium in order to demonstrate the advantage of SOI + MEMS for the FEM.

Countries: Canada, France, South-Korea, Sweden

Partners:

Canada	Université Quebec Trois Rivières
France	ACCO, CEA-LETI, Coventor, STMicroelectronics, Uni EpOC-UNS, Uni Grenoble-INP
South-Korea	KAIST, SEMCO
Sweden	ACREO, Ericsson

Expected Start Date: 01-03-2014
Expected End Date: 28-02-2017

3.1.3. Project CT217 RESIST

Resilient Integrated Systems

Project leader: Maurice Meijer (NXP-NL)

Brief description:

Electronic systems in cars and planes are becoming more sophisticated and demand more integration and higher performance from semiconductors. However, it is well-recognized that lifetime degradation induced by scaled down technologies will threaten the integration of highly reliable and safety critical systems due to the usage of scaled down products. Hence, this motivates the need for new reliability aware design approaches and solutions.

The RESIST project targets reliability aware design methods and run-time adaptive approaches for next-generation resilient integrated electronic systems in Automotive and Avionics. The focus is on reliability, cost-effectiveness and quality of semiconductor devices. The consortium consists of semiconductor companies, SME's, academia, institutes, and end users. Expected benefits target to exceed 2 times more cost-effective resilience solutions, 25 years lifetime of embedded devices, 20% higher component/integration density at the same level of reliability and up to 30% reduced reliability testing costs. An early-warning system by health monitoring of system components will be developed.

Countries: France, Germany, The Netherlands

Partners:

France	Atmel, IROC, STMicroelectronics, CEA-LIST, Grenoble-INP, ISEN Toulon, *subcontractor:* IPPON

Germany	Bosch, EADS, Infineon, MunEDA, NXP, Volkswagen, Fraunhofer IIS/EAS, Reutlingen University, TU-Munchen, TU-Bremen ITEM
The Netherlands	NXP, Heliox, TU-Delft, TU-Eindhoven

Expected Start Date: 01-07-2014
Expected End Date: 30-06-2017

3.1.4. Project CT218 E450LMDAP - *ENIAC Project co-labelled*

European 450mm Lithography and Metrology Development for Advanced Patterning

Project leader: Gerold Alberga (ASML)

Brief description:

The overall goal of the E450LMDAP project is to develop 450mm lithography and metrology modules and tools and to initiate distributed pilot line activities over the 450mm lithography and metrology tool platform eco system. These pilot line activities will complement the activities from the already initiated ENIAC JU E450EDL project.

In addition, also early 450mm wafer 1x node advanced patterning process development at the IMEC's pilot line will be part of the project. Lithography, Metrology and deposition equipment performance suited for 450mm will be demonstrated in the IMEC pilot line, interconnected with holistic methodologies to the 450mm pilot line at IMEC which is equipped with European systems.

The project will complement the engagement of the European semiconductor equipment industry in the 450mm wafer size transition that started with the ENIAC JU EEMI450 initiative and proceeded with subsequent projects funded with public money, amongst others NGC450, SOI450, EEM450PR and E450EDL which will result into first critical process module availability in the IMEC pilot line.

The consortium comprises 44 members from 7 different European countries with SMEs and research institutes and also IDM as end users. The project is organized in three technical work packages and a work package on management and coordination.

The main objective in the work package on lithography is to develop and to have prototyping activities comprising amongst others wafer stage, wafer handler, optics, electronic as well as preliminary tool system qualification.

In the dedicated work package on metrology 450mm metrology tool types will be developed for wafer and mask platforms as well as a holistic metrology data hub for advance lithography data management and fab.

Finally, in the work package on advanced patterning a selection of critical N10 layers, which are currently under development at 300mm wafer sizes, will be transferred to an early 450mm lithography platform.

Countries: Belgium, France, Germany, Ireland, Israel, The Netherlands, United Kingdom

Partners:

Belgium	ASM, ASML, IMEC
France	ADIXEN, CEA-LETI, Coventor, ECP, IPPON, LTM-CNRS, RECIF, STMicroelectronics
Germany	AMTC, ASYS, BG, Bosch, GF, IDE, SemiLev, Toppan, Zeiss SMS, Zeiss SMT
Ireland	NN2
Israel	AMIL, NN1, JVS, KLA-Tencor, Nanomotion, Nova, Zeiss Karmiel
The Netherlands	ASML, AAE, Benchmark, Bosch, CCM, Irmato, KMVE, Neways, Prodrive, Reden, Segula, TNO, TU-Delft, VDL-ETG
United Kingdom	Oxford Instruments

Expected Start Date: 01-10-2014
Expected End Date: 30-09-2017

3.1.5. Project CA114 WiCon

Non-Galvanic Contactless Connectors for Power and Data Transfer

Project leader: Cicero Vaucher (NXP)

Brief description:

The WiCon project will provide low-cost, highly-integrated system solutions for galvanic connector's replacement in the consumer and industrial market segments. Smart electronic systems for data and power transfer will be demonstrated, exploiting ultra-low-power point-to-point mmWave connections and optimized power transfer technologies merging NFC with wireless charging applications. In addition, polymer waveguides carrying mmWave signals for data-transfer rates above 20Gbps will be demonstrated, as a low-cost replacement option for expensive optical components in the next-generation 10Gbit USB standard and above.

Countries: Belgium, Finland, France, The Netherlands

Partners:

Belgium	KUL, NXP
Finland	VTT, Nokia, Pulse Finland Oy
France	Archos, NXP, nearforge, Cassidian
The Netherlands	NXP, Tyco Electronics, DUT

Expected Start Date: 01-04-2014
Expected End Date: 31-03-2017

3.1.6. Project CA116 CORTIF

Coexistence Of RF Transmissions In the Future

Project leader: Dominique Défossez (NXP)

Brief description:

The CORTIF project aims is intended to at optimise the coexistence concurrent exploitation of radio frequencies by multiple communicating devices in a world where there are increasing demands on available RF spectrum of concurrency frequencies bands. It is applicable across distances of different orders of magnitude; from a single PCB out to the wide area with radios that might be far apart. CORTIF will exploit the trade-offs that are possible by working across layers of the communication stack and will address both the application and technology layers. Mobile, Set-Top Box and TV makers will define the system requirements constraints; semiconductors suppliers and integrators will develop the coexistence techniques strategies taking into account considering the RRF standardization activity, the power consumption, permissible error rates and, of course, the bill of materials. Assembling such a wide range of expertise from application developers to semiconductor designers, standards experts to software developers, is only possible in a large, multinational, multi-specialism project such as that enabled by CATRENE.

Countries: Austria, Czech Republic, France, The Netherlands, Portugal, Spain, Turkey

Partners:

Austria	Uni. of Applied Science of Upper, Austria, Lantiq, ARCOSIC Research
Czech Republic	Brno UoT, IMA
France	XLIM Xlim, Institue Mines-Telecom, NXP, Technicolor, Cassidian
The Netherlands	TU-Eindhoven, Technolution, Imec, NXP
Portugal	Instituto de Telecomunicacoes, GSLDA
Spain	iquadrat
Turkey	Mikroelektronik Arastirma Gelestirme Tasarim ve Ticaret

Expected Start Date: 01-01-2014
Expected End Date: 31-12-2016

3.1.7. Project CA118 FITNESS

Full Integrated Transceiver for Next generation Emergency ServiceS

Project leader: Sami Aissa (Cassidian)

Brief description:

FITNESS aims at preparing the future of Professional Mobile Radio (PMR) in Europe and in the world. It paves the way towards high performance PMR based on Long-Term Evolution (LTE) and new functionalities requested by mission critical markets, while preserving backwards compatibility with existing PMR systems. It exploits the progress done in integration and signal treatment domains, using the CATRENE cluster to make organisations specialized in key domains work together to develop a versatile and multistandard platform. FITNESS delivers innovative PMR architecture taking into account RF standardisation activity, radio coverage, power consumption and the bill of materials.

Countries: France, Portugal, Spain, Turkey

Partners:

France	Cassidian, ISEP, IMS lab, Be Spoon, NXP, CEA-Leti, Ecole Centrale de Lyon, Telecom Bretagne
Portugal	Instituto de Telecomunicacoes, GSLDA
Spain	iquadrat
Turkey	Mikroelektronik Arastirma Gelestirme Tasarim ve Ticaret

Expected Start Date: 01-10-2014
Expected End Date: 31-03-2017

3.1.8. Project CA208 MobiTrust

Trusted Mobile Platforms

Project leader: Jean-Pierre Tual (Gemalto)

Brief description:

The general objective of the MobiTrust project is to develop a complete embedded framework (HW, SW mechanisms and related management, HW/SW forensics tools) aimed at enhancing the security and privacy protection of future mobile platforms such as smartphones or Tablets running over open platforms such as Android or Win8. These mechanisms will target primarily new usages of such devices, supporting some major trends in enhanced mobility both in the Consumer/Enterprise (BYOD), Smart-City and Civil Security, Mobile Cloud, Massive On-Line Open Courses (MOOC).

Countries: Austria, France, Germany, Portugal, Spain.

Partners:

Austria	Infineon, Graz UoT
France	Trustonic, CEA-Leti, Cassidian, Gemalto, NXP, Archos, CryptoExperts, Trusted Labs
Germany	Fraunhofer, NXP, Infineon
Portugal	CMSF, OneSource, Instituto de Telecomunicacoes
Spain	Uni of Cantabria, Banco Santander, TST, iquadrat

Expected Start Date: 01-04-2014
Expected End Date: 30-09-2016

3.1.9. Project CA405 INSIGHT

Intelligent Sensor Fusion for Instrument Guidance and Human Safety

Project leader: Robert Hofsink (Philips)

Brief description:

In many complex, safety critical, environments there is a growing need for supervision and accurate guidance of objects in that scene to improve safety and drastically ease the workflow. Examples: - *Medical:* instrument guidance, room safety - *Security and surveillance:* facial surveillance, behaviour analytics. Given the complexity of the required task, a single sensor solution is in many cases not sufficient to achieve this goal. For this goal the INSIGHT project will develop intelligent multi sensor fusion technologies to realize the required supervision and guidance.

Countries: Belgium, Finland, The Netherlands

Partners:

Belgium	UoG, Easics, Xenics, eSATURNUS
Finland	VTT, Teleste, RikolaSPECIM
The Netherlands	TU-Eindhoven, Philips, Microflown AVISA, BOSCH, ViNotion

Expected Start Date: 01-04-2014
Expected End Date: 01-04-2017

3.1.10. Project CA507 GREETINGS16

Green Computing 2016

Project leader: Patrick Blouet
(STMicroelectronics)

Brief description:

The aim of Greeting16 is to deliver an innovative high-density, energy-efficient computing solution for embedded and cloud computing applications. Modern data centre Total Cost of Ownership (TCO) is increasingly accounted for by equipment operating expenses, mainly energy costs, rather than capital costs. An important goal of Greeting16 is to create a truly European vertical solution to this problem, also tackling the distinct lack of European key technologies and a lack of knowledge in system integration. Greeting16 will leverage European strengths in embedded systems and software, and help ensure that technology developed in European labs, including FDSOI, 3D stacking, NVM and silicon photonics, together with the 64-bit ARMv8 architecture, will be translated into highly-competitive European server products with high density form factor and low energy demand. Off-loading of signal-processsing tasks (e.g. image analysis) tasks to programmable accelerators will boost energy efficiency further. In order to provide a comprehensive utilization of the new FDSOI technology a tight link to the software layers is needed. This is an important prerequisite in order to optimize the benefits of the new FDSOI technology in contrast to standard CMOS. Therefore, we will also leverage the long track record in Europe regarding the software industry, in order to provide a complete solution tightly integrating the hardware and software components. Involvement of key European players in the Linaro foundation, for instance, demonstrates the capacity of the project to develop a complete solution, providing the best fit between the software and the underlying hardware.

Countries: France, Germany, Greece, The Netherlands, Portugal, Spain, Sweden, Turkey

Partners:

France	PEERGREEN, STMicroelectronics, Université Jean Monnet, Magillem Design Services, Thales, CEA-Leti, Universite Joseph Fourier, TIMA
Germany	Wincor Nixdorf, FZI, University of Tübingen, VI Systems, University of Paderborn, TU of Kaiserslautern, AEMtec, Fujitsu Technology Solutions, SUSE LINUX, EXTOLL
Greece	Foundation for Research and Technology-Hellas
The Netherlands	ViNotion, TU-Eindhoven, ST-Ericsson
Portugal	GSLDA, University of Minho, University of Aveiro, Instituto de Telecomunicacoes
Spain	iquadrat
Sweden	Chalmers University of Technology
Turkey	TUBITAK-BILGEM, Sabanci University

Expected Start Date: 01-01-2014
Expected End Date: 31-12-2017

3.2 Projects ended in 2013

3.2.1. Project CT205 REFINED

Renewed Embedded Flash and other Innovative NVM for Extended Domains of application

Project leader: Dominique Goubier
(STMicroelectronics)

Brief description:

The REFINED project has created technological advantage and thereby adding value to European technology and products through development of embedded non-volatile memory in sub-90nm CMOS technology and also providing cost effective solutions for those qualified technologies. During the 3 years period significant achievements were made even if during the same period, the overall semiconductor industry has faced some very challenging periods. Regarding the achievements, all the project milestones were met even if some target nodes has been fine tuned to fit with market evolution.

The ST 55nm eFlash technology has passed the qualifications steps successfully and is ready for production as well as the preliminary work for the development of the 40nm new floating gate memory. For ATMEL, 3 eFlash technologies (from 90nm to 150nm) are in the production phase and a roadmap has been defined for the 65nm embedded memories. LFoundry is going on with the plan to run in parallel the development of the LF110 CMOS core process with 2 embedded memories options (SST and single poly NVM). The Italian partners of the project were not funded at all. Nevertheless, ST-Agrate maintains his effort in areas where there is direct dependence of deliverables with the other partners in order not to jeopardize the overall program progress.

Countries: Starting with 4 countries (France, Germany, Italy, The Netherlands) and ending with only 3 (France, Germany, Italy).

Partners:

France	Atmel, LFoundry, CEA-LETI, STMicroelectronics
Germany	Infineon
Italy	STMicroelectronics

Start Date: 01-01-2010
End Date: 31-12-2012

3.2.2. Project CT206 UTTERMOST

UlTimaTe EnablemenT Research on 32/28NM Cmos Technologies

Project leader: Gilles Thomas
(STMicroelectronics)

Brief description:

The activities of the 19 partners involved in UTTERMOST during the full length of the project had the goal to unite the 3 European industrial companies' member of the ISDA Alliance for the complete development of CMOS technology platforms at 32 and 28nm with the realization of the design of 4 demonstrator circuits. The achievements are divided into 3 main thematic along the different Work Packages. WP1 to WP5 were devoted to technology development and implementation in the Fabs, WP6 & WP7 were related to the design enablement initially at 32nm and then at 28nm while WP8 was dedicated to the design/verification of the 4 circuit demonstrators.

During 2010/2011 the project was focused on 32nm while during the ending period (2012/13) the project focus switched to the 28nm design enablement, process qualification and validation of demonstrators. Globally the project milestones have been satisfactorily completed by all partners. UoS and ALU-D were authorized through CR4 to complete their task by end of 2013. The qualification (industrial maturity) of the 28nm LP technology at ST Crolles2 fab was achieved concurrently with the project. The 32nm and 28nm technologies reached respectively all their targets in term of device performance and integration density as well as reliability. The design platforms met their targets in term of dynamic and static power as well as speed allowing the complex demonstrators to prove the benefits of the technology. Such complex demonstrators were not achievable with previous technology nodes. Industrial exploitation of the 32nm and more recently of 28nm technology platform has already started successfully. UTTERMOST was key project to install in EUROPE:

- A 32nm digital CMOS design platform and design enablement (at ST);
- A 28nm digital CMOS design platform and design enablement (at ST& IMC);
- A site for prototyping and industrialization of a 28nm bulk LP CMOS using HK/MG gate first and novel BEOL for up to 10 ML. A second source plant at GF was qualified.

The learning curve of the 28nm LP technology was instrumental for developing the 28nm FDSOI technology and the conversion methodology from 28nm LP to 28nm FDSOI including the porting of the 28LP libraries.

Countries: France, Germany

Partners:

France	STMicroelectronics, Intel Mobile Communications, Dolphin, ST-Ericsson, TCF, CEA-LETI, CEA-INAC, CAMECA, SERMA, Grenoble INO-IMEP, CNRS-LTM, CNRS-CEMES, IBS
Germany	Intel Mobile Communications, Alcatel-Lucent, Fraunhofer IIS/EAS, Fraunhofer IIS/B, University of Stuttgart, Global Foundries (Unfunded Partner)

Start Date: 01-06-2010
End Date: 31-05-2013

3.2.3. Project CT207 COCOA

Chip-On-Chip technology to Open new Applications

Project leader: Brigitte Descouts (STMicroelectronics)

Brief description:

For decades, Moore's law has predictably driven silicon scaling, and semiconductor manufacturing has been based largely on planar (2D) technology. But the increasing need for lower power, smaller form factor and higher performances continues to drive ICs to 2.5D and 3D. COCOA project was fitting exactly with this approach by gathering the expertise of industrials and laboratories around a common objective: develop a complete mature 3D integration technology platform covering the entire range of processes required from vertical interconnects (TSV, micro bumps…) and robust bonding to innovative packaging approaches to address a wide range of products.

COCOA results specifically highlighted:

1. 3D interconnects shrink and the associated specific development process steps to increase density and cover the existing gap between medium (104 cm-2) and high density (106 cm-2) technologies,
2. 3D performance (thermal, mechanical, electrical…) improvement,
3. Realization of product demonstrators: Specific prototypes are developed for multimedia and wireless applications as well as for sensor integration applications that open new tremendous manufacturing opportunity to European partners.

The project started 01 March 2010. An extension of four months allowed all partners to pursue their collaboration up to 30 June 2013. A further six months extension (up to end 2013) for partners AMS, SPTS and BESI has been necessary to allow the finalization of the sensor demonstrator. The first real 3D integration of a processor with a wide IO memory interface has been published in 2012 with excellent electrical results. Some of the very challenging steps for sensor integration with a µhot plate were achieved. One of the major 3D integration challenges, i.e. the bonding and debonding steps for thin wafers, was successfully developed and demonstrated using standard alignment equipment. The dissemination activity was also a major point of the project with about 70 publications and 12 patents.

Countries: Austria, Belgium, France, United Kingdom

Partners:

Austria	AIT, ams, BESI, EVG, TU-Wien
Belgium	ASM
France	STMicroelectronics (Crolles + Tours), ST-Ericsson, CEA-LETI, IM2NP, AMAT
United Kingdom	SPTS

Start Date: 01-03-2010
End Date: 30-06-2013 + 6 month extension for Austrian Partners

3.2.4. Project CA104 COBRA

Computing Fabric for High Performance Applications

Project leaders: Philppe Garcin (STMicroelectronics), Kees van Berkel (Ericsson) (2013)

Brief description:

Hardwired SoC architectures suffer from a lack of flexibility regarding market evolution, resulting in an excessive design cycle time and increased cost.

Furthermore, process variability is not yet well addressed for 32nm and beyond. The objective of COBRA is to develop and experiment an open, flexible and high performance platform based on a regular array of processors. The platform is driven by Automotive, Radio and Video benchmark applications.

The main result of the project is the whole development (until demonstration) of an open, flexible and high performance platform based on a regular array of processors running in parallel. This ambitious objective required the definition of an ad hoc architecture, and a strong effort at design automation level. The main difficulty to overcome was probably the integration constraints when one has to integrate a hierarchy of computing resources with a set of embedded software and run-time

functions. Most of the partners had a double expertize, both in hardware and software. However, thanks to the level of automation provided by COBRA, designers with only software knowledge will be able to get efficient hardware/software implementations realized.

The COBRA platform is composed of clusters of 17 processors. The silicon demonstrator realized during the project includes 4 clusters. This is only an example of implementation, the number of clusters being quite flexible. This demonstrator reaches 80 GFLOPS for less than 2 watts. One has to be careful before to generalize metrics, but it is very encouraging to note that ARM Cortex-A9 or NvidiaTegra3 each propose a solution with a computing power per watt 10 times smaller. Many partners – if not all – provided improvements in terms of performance, through very various techniques (optimizing compilers for code speed, optimizing memory bandwidth etc). Time-to-Market tends to explode when a parallel application has to be built (and programmed!). This is why the project proposed three simulation/emulation platforms (TLM, RTL, FPGA) allowing first architectural choices to be done very fast. As part of this offer, a simulation platform using inter-processor communication allows a 5x to 10x acceleration factor. Power consumption (especially when Mobile Applications market is at stake) was permanently cared about, and energy saving Voltage Scaling policies are part of the outcomes. For example, different “power modes” are available from processor level to Processing Array (which benefits from a hierarchical unit called CVP, Controller of Variability and Power). For each application, COBRA platform allow to choose the most adapted trade-off between performance and power consumption. Of course, whenever a new control is proposed as an add-on (and there are many), one tries to minimize its consumption and area overheads. Yield is still another parameter which will benefit from the inherent redundancy from COBRA homogeneous architecture.

Countries: France, The Netherlands, Spain

Partners:

France	Caps Enterprise, CEA, STMicroelectronics
The Netherlands	ST-Ericsson, Compaan Design, ACE, TU-Eindhoven, TU-Delft, NXP, Synopsys
Spain	University of Cantabria, University of Barcelona, Tedesys Global, Ecomunicat Electronics, Marvell, Vista-Silicon, Sapec

Start Date: 01-01-2010
End Date: 31-12-2013

3.2.5. Project CA202 eGo

Easily connected to the world

Project leader: Christian Dietrich (Gemalto)

Brief description:

The CATRENE eGo project represents an innovative way to enable users for a secure, seamless and privacy-keeping way of interacting wirelessly within the emerging world of the Internet of Things and more generally to manage their digital interactions in a more and more connected world. The initial eGo concept is based on the most natural and intuitive interaction people can have with objects, just by touching them, hence bootstrapping a bidirectional communication (UWB, Zigbee,..) between a user-worn device and the object via a Body Coupling Communication interface, where the object plays the role of emitter and the Human skin the one of receiver.

The project resulted in an enthusiastic cooperation experiment undertaken by 11 partners from France, Ireland, Sweden, and Norway, from 30 June 2010 to 31 December 2013. By the project end, the following significant results have been achieved:

- Prototypes of wearable devices incorporating the various versions of the eGo proof of concepts with the key electronic SoC developed in the project (UWB controller, protocol processor, BCC controller) have been made available. The evaluation made through the target project demonstrators proved that these advanced technology components are meeting the expected performance/cost characteristics needed to develop pre-series of appropriate eGo devices matching the requirements of wearable devices in several application domains.
- Several demonstrators from four different application domains have been shown by the end of the project, validating all key system characteristics of the eGo concept. From these demonstrators, implementation guidelines and reference implementations useful for further market developments can be derived.
- 20 patents have been submitted over the project life-time, paving the way for the project standardization strategy.
- Based on the technical results and IP effort described before, the eGo project standardization process has entered now a new phase as contributions specific to the eGo technology (UWB MAC/LINK layers) are ready to be submitted to the ETSI Smart-BAN standardisation working group from early 2014. This should give to the European Industry some strong foundations for entering the emerging IoT and wearable device market
- Innovative strong authentication and anonymity preserving protocols have been developed and implemented in the project, making the eGo concept both secure and privacy-preserving for managing digital interactions in the new IoT world.
- Several of the projects results are ready for full commercialization, including the DecaWave UWB SoC, the latest chip from the ST32 family (ST32L4 SoC) developed in the project, a new patent-protected Idex fingerprint sensor, the Precise Biometrics Match on card technology. Gemalto is also in contact with some financial and telecom operators to launch some pre-series to test the market acceptance of the eGo technology. ATOS Worldline (now Worldline) and Continental are also looking for commercial exploitation, but will need respectively simpler architecture in the payment context and better technology stability for the automotive domain. Tyndall is finally ready to provide reference implementation to the Irish SME community and CIT will continue enhancing their results in the context of the Nimbus Labs.
- The project has been recognized through several awards during its lifetime; during the last year, the eGo payment demonstrator has been awarded by the 2013 Innovative Payments Trophy in the "e-commerce products" category at the PayForum fair in Paris, and the DecaWave UWB chip with RTLS capabilities has been nominated as one of the 100 Hot products (Wireless category) of the year by EDN and got also the ICS New Product Innovation Leadership Award 2014 from Frost & Sullivan. This adds-up to other awards received in 2011 and 2012.

- About 15 project presentations have been made during conferences or exhibitions and in total the project has been cited in more than 100 International Press references.

Countries: France, Ireland, Norway, Sweden

Partners:

France	Atos Worldline, Gemalto, STMicroelectronics, INRIA, Continental
Ireland	Institute of Technology Cork, Tyndall National Institute, Decawave, Lincor Solutions
Norway	IDEX ASA
Sweden	Precise Biometrics

Start Date: 01-07-2010
End Date: 31-12-2013

3.2.6. Project CA502 SEEL

Solutions for Energy Efficient Lighting

Project leader: René de Zwart (Philips)

Brief description:

European governments are fading out all incandescent light bulbs and low-efficiency halogen bulbs from the market. Lighting companies continuously look to improve the energy efficiency of the lamps. HID lamps (High Intensity Discharge lamps) and SSL (Solid State Lighting) based light sources will boost the efficacy of the system typically by a factor five. This will lead to tremendous energy consumption reductions and consequently reduced CO_2 emission. Such lighting systems need to meet the requirements of halogen systems which are applied in general lighting and automotive applications. To achieve this goal, European specialists in lighting, automotive, electronics, controls, and semiconductors teamed up with application partners in the CATRENE project SEEL (Solutions for Energy Efficient Lighting) which ended on 31 October 2013.

The project played an important role in the two major trends in the lighting industry:

- "LEDification": the change from traditional lighting to the more energy efficient LED lighting;
- "SMARTification": the introduction of smart lighting controls to enable switching off unnecessary lighting.

The project with a consortium of four European countries contributed to strengthening the position of Europe as a worldwide knowledge centre and enlarged the competitive position of Europe in the world, in particular for lighting.

SSL general lighting has chosen the optical concept for a high lumen LED spot module to achieve a breakthrough architecture with regard to dimensions (8mm height, 10x10 cm surface for 5000 lm), light quality (CRI80 & CRI 90, CCT from 2700 to 5000K, beam shaping) and cooling needs (active and passive cooling). The major technology step taken was the proven use of transfer moulding technology to realize multiple silicone domes onto the LEDs mounted on a PCB. The aspect ratio of the moulded lenses as achieved in the SEEL project has not been shown before.

For HID general lighting, a compact hot restrike system was implemented, thereby extending the application range of HID technology. Innovations in all system components, lamp, fit system and control gear have been combined to cut in half the necessary voltage level, optimize insulation properties and minimize tolerances.

To control lights depending on the position and walking direction of people in a room, an innovative low-cost presence detection sensor filling the gap between PIR and IR imagers has been developed. It is based on thermal infrared microbolometer imaging technology. The newly developed sensor detects presence and motion by picking up the heat emitted by the human body. The algorithm is directly implemented in the detection part of the sensor and the output is generated using semantic descriptions, preserving privacy. The lights are controlled wirelessly using WiFi.

Concerning the SSL automotive intelligent headlamp, the chosen electric architecture with LEDs wired in parallel has proven to enable densely packed and fully addressable LED arrays with superior thermal transport. The parallel approach was the key item to realize the main project target i.e. typical operation at a board temperature of 150°C to account for thermal environments seen in engine compartments. Additionally, the architecture offers a high degree of modularity, i.e. the team was able to operate all headlamp functions based on a high diversity of LEDs with identical controls/driver.

For HID automotive lighting, a significant reduction of the ignition voltage was realized using an improved ignition aid for the burner to come to a less expensive HID system as a replacement of halogen lamps in smaller cars too.

New generation of lighting systems which include intelligent lighting control developed in the SEEL project, is support global energy savings without sacrificing the well-accepted properties of existing lighting solutions. Standardization regarding both light source and intelligent control will enable to reach high volume applications, based on a substitution of existing lighting market. By increasing the volume demand, standardization will also enable to conduct cost reduction at light sources and system control level, as well as securing a leading position for the European lighting industry now and in the future.

Countries: Belgium, France, Germany, The Netherlands

Partners:

Belgium	Philips, PITS
France	ULIS, Philips, Valeo Vision, CEA-Leti,
Germany	Osram, Bender+Wirth, Audi, Infineon, Elmos Semiconductor, Fraunhofer-IZM, Philips, BAG Electronics, BJB, NXP, Ruhr University Bochum
The Netherlands	Philips, TU-Eindhoven, BIC Industries, DCD Technology, NXP, TU-Delft, BE Semiconductor Industries

Start Date: 01-11-2010
End Date: 31-10-2013

4

Appendix A
CATRENE
Projects Focus Matrix

Appendix A. CATRENE Projects Focus Matrix

The CATRENE Projects Focus Matrix identifies the work areas addressed by each project. A maximum of 5 *s can be allocated to a single project. A * indicates that the project addresses the work area in question, with this focus growing with each additional *.

PROJECT NAME	Communication & Digital Lifestyle	Safety & Security	Automotive & Transport	Health and the Ageing Society	Energy Efficiency	Design Technologies	Semiconductor Process & Integration	Equipment, Materials & Manufacturing
CA101 PANAMA	**				*			
CA103 HERTZ	**				*			
CA104 COBRA	***					*		
CA109 SHARP	*			*		***		
CA110 APPSGATE	**			*	*			
CA111 UltraHD-4U	***							
CA112 HARP	**		*		*	*		
CA114 WiCon	***						**	
CA116 CORTIF	***							
CA118 FITNESS	***					**		
CA202 eGo	*	***						
CA206 NewP@ss		***						
CA208 MobiTrust		***						
CA301 HiDRaLoN	*		*	*				
CA303 OPTIMISE			**		*	**		
CA308 ICAF	***	**						
CA310 EM4EM			***			**		
CA402 THOR			*	*	*	*		
CA403 RELY			*	*		***		
CA405 INSIGHT		**		**				
CA501 COMCAS	**				**	*		
CA502 SEEL			**		***			
CA505 BENEFIC	*				**	**		
CA507 GREETINGS16					***	**		
CA701 H-INCEPTION						***		
CA703 OpenES	*		*			***		
CT105 3DIM3	*					**	*	
CT204 PASTEUR				*			***	
CT205 REFINED						*	***	
CT206 UTTERMOST						*	***	
CT207 COCOA						*	**	*
CT208 REACHING 22						**	**	
CT209 RF2T4Z SISOC	*					*	***	
CT210 DYNAMIC-ULP	*					**	*	
CT213 3DFF				*	*	*	**	
CT215 SMART FE	**						**	*
CT217 RESIST			**			***		
CT218 E450LMDAP								***

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PROJECT NAME	Communication & Digital Lifestyle	Safety & Security	Automotive & Transport	Health and the Ageing Society	Energy Efficiency	Design Technologies	Semiconductor Process & Integration	Equipment, Materials & Manufacturing
CT301 EXEPT								***
CT302 TOETS								***
CT305 SOI 450								***
CT306 NGC 450								***
CT312 MASTER_3D								***
CT315 EmPower			*		**		*	
CT402 9D-Sense		*		*		*	**	

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Appendix B
Glossary of Terms

Abbreviation	Description
AENEAS	Association for European Nanoelectronics Activities
BEOL	Back End of the Line
BOM	Bill of Materials
CATRENE	Cluster for Application and Technology Research in Europe on Nanoelectronics
CMOS	Complementary Metal Oxide Semiconductor
CVP	Controller of Variability and Power
DTC	Design Technology Conference
ECSEL JU	Electronic Component and Systems for European Leadership Joint Undertaking
EDA	Electronic Design Automation
EMC	Electro Magnetic Coupling
EMI	Electro Magnetic Interface
FDSOI	Fully Depleted Silicon on Insulator
FEM	Front End Module
FP	Full Proposal
FP7	Seventh Framework Programme
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
Gbit	Gigabit
Gbps	Gigabit per second
GFLOPS	Giga FLoating-point Operations Per Second
HID	High-Intensity Discharge
HK/MG	High-K/Metal Gate

Abbreviation	Description
HW	Hard Ware
I/O	Input/Output
IC	Integrated Circuit
IDM	Integrated Device Manufacturer
IoT	Internet of Things
ISDA	International Semiconductor Development Alliance
LP	Low Power
LTE	Long-Term Evolution
MASP	Multi-Annual Strategic Plan
MEMS	Micro-Electro-Mechanical Systems
MOOC	Massive On-Line Open Courses
NFC	Near Field Communication
nm	nanometer
NVM	Non-Volatile Memory
PCB	Printed Circuit Board
PMR	Professional Mobile Radio
PO	Project Outline
PY	Person Year
R&D&I	Research, Development and Innovation
RF	Radio Frequency
RFF	Radio Related Functions
RFMEMS	Radio Frequency Micro-electro-mechanical systems

Abbreviation	Description
RTL	Register Transfer Level
RTLS	Real-Time Locating System
Si	Silicon
SiC	Silicon Carbide
SoC	System on a Chip
SOI	Silicon on Insulator
SSL	Solid State Lighting
SST	Silicon Storage Technology
SW	Soft Ware
TCO	Total Cost of Ownership
TLM	Transaction Level Modelling
TSV	Through-Silicon-Via
USB	Universal Storage Bus
UWB	Ultra Wide Band
VMS	Vision Mission Strategy
WiFi	Wireless Fidelity
WP	Work Package

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