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Project Result Sheets

Cluster for Application and Technology Research in Europe on NanoElectronics

EUREKA Cluster for Application and Technology Research in Europe on NanoElectronics

CATRENE

Project Profiles and Result Sheets

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E450LMDAP is a co-labellled project with ENIAC JU.
For more information on this project,
please see www.eniac.eu.

CALL 1

Cluster for Application and Technology Research in Europe on NanoElectronics

CA101 | Attending to core technological issues helps ensure future success of mobile communications [PANAMA]

As the use of mobile phones, especially the smart variants, grows from strength to strength with increased subscribers chasing even more functionality, capacity and performance, behind-the-scenes issues relating to networks and handsets need to be addressed if this momentum is to be sustained. That's where PANAMA comes into its own. This project has successfully exploited the expertise and experience of leading European partners from the semiconductor, test tools, electronic design automation industries, and academic institutions in dealing with critical issues. This collaboration between industry and academia also demonstrated the value universities, with their wealth of knowledge and research resources, can bring to a partnership, something entrepreneurs on both sides are taking advantage of.

PANAMA brought together a large consortium of project partners with specialist expertise, from various industries, such as semiconductor, test tools and electronic design automation, but also from academia. They focused on a wide range of advanced application areas and systems (integrated, discrete and distributed), such as multi-band, multi-mode and more efficient power amplifiers and transmitter systems for mobile handsets, as well as, base transceiver stations, avionics, mobile satellite communication and home networking.

Project activities included:

- Designing and developing key components,
- Improving system efficiency,
- Developing standards and design methodology,
- Developing models and simulation and characterisation tools,
- Promoting PANAMA and disseminating project results/achievements through the internet, scientific publications, and workshops and conferences.

Surpassed initial goals

Clear project goals were assigned at the start:

- 20% efficiency improvement for integrated systems,
- 30% efficiency improvement for discrete systems,
- 10% efficiency improvement for distributed systems.

All tasks were completed on time, deliverables achieved and initial goals met. What is more, techniques (developed or optimised) relating to integrated and discrete systems – 2G/3G mobile applications, home networking, base stations, airborne and satellite communications – even surpassed initial targets.

Good project-participation mix

A fine example of pan-European collaboration, PANAMA was a strongly industry-focused project that attracted more than 20 participants from five countries, and where universities played an important role in resolving 'roadblocks'.

In line with other CATRENE projects, PANAMA's activities, tasks and deliverables were divided into 'work packages' (WPs), to which project partners were assigned based on their skills and expertise. Notably, WP4 provided the tools essential to the activities in other WPs.

Internal collaboration was excellent, ensuring a smooth and successful operation. A sign of good co-operation and engagement among partners was reflected in the high attendance at project review

ENERGY-EFFICIENT DEVICES AND ENERGY CONTROL SYSTEMS

Partners:

Agilent Technologies Belgium
Amcad Engineering
CEA-LETI
ELTA Systems
ESIEE Paris
Gigle Semiconductor
IEMN
IMS
Institut Telecom
KU Leuven
MC²
NXP Semiconductors FRA, NLD
OMP
ST-Ericsson Belgium
STMicroelectronics
THALES Communications
TNO
TU Delft
TU Eindhoven
UPC-HiPICS

Project leader:

Philippe Meunier
NXP Semiconductors

Key project dates:

Start: January 2009
End: September 2012

Countries involved:

Belgium
France
Israel
The Netherlands
Spain

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✓
Digital lifestyle	✓
Design technology	
Sensors and actuators	
Process development	
Manufacturing science	
More than Moore	✓
More Moore	

meetings. This was also reflected in the number of joint publications (many involving partners from industry and academia) and patents, as well as, workshops organised by and for project members.

Putting PANAMA's deliverables to good use

Most importantly, PANAMA will offer mobile users handsets with batteries that are even more energy-efficient, as well as, faster, higher-capacity internet connections, with even more access-points. This also means that service providers will have satisfied clients with an even greater appetite for mobile and web services.

Behind the scenes, PANAMA delivered, first and foremost, tools needed to support its own project activities. The nonlinear characterization tools led to faster and more automated and accurate measurement-taking and harmonic matching, as well as, support for low- and high-power for devices under test, new measurement possibilities and with higher frequency. Importantly, these tools did not require the normal high-level of expertise to operate them.

Nonlinear models developed were more accurate. Thanks to improved extracted models, a Power-added Efficiency increase of 10%-15% was achieved and model extraction simplified. Simulation tools increased functionality and performance, surmounting current limitations.

Then there were deliverables whose benefits went beyond the project boundaries. A new architecture and design methodology developed in PANAMA will lead to future improvements in transmission efficiency. From an academic point of view, universities and research laboratories increased their expertise through the 15 PhD students trained in PANAMA, the three patents issued, and the 137 papers published in prestigious journals or presented at international conferences. And standards established during joint-development work developed by NXP and TU Eindhoven on Beamformer and down-tilt antenna for base stations have been submitted for acceptance to the international Antenna Interface Standards Group, AISG, of which NXP is member.

Some deliverables and contacts even had commercial consequences outside the actual project. Firstly, a start-up, Anteverta-mW BV, was created by TU Delft to commercialize the active harmonic load-pull test setup developed in the project. And the first customer was a PANAMA partner, NXP.

Next, the transfer of expertise from academic partner to industry is also going well. More generally, there are several cases where architectures and circuit components developed through the collaboration between university and industry are being deployed by the industry partner.

Finally, to quantify the accuracy of the measurements using the nonlinear characterizations tool benches, IEMN developed a nonlinear reference component called the 'Golden Device'. It is capable of quantifying the accuracy of nonlinear measurements, and is currently being used by other European laboratories.

Looking to the future, PANAMA's innovative deliverables and other project output are also available to European integrated circuit (IC) manufacturers and system providers, for example, and can be deployed as part of their defence against external competition.

CATRENE
Cluster for Application and Technology Research in Europe on NanoElectronics

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

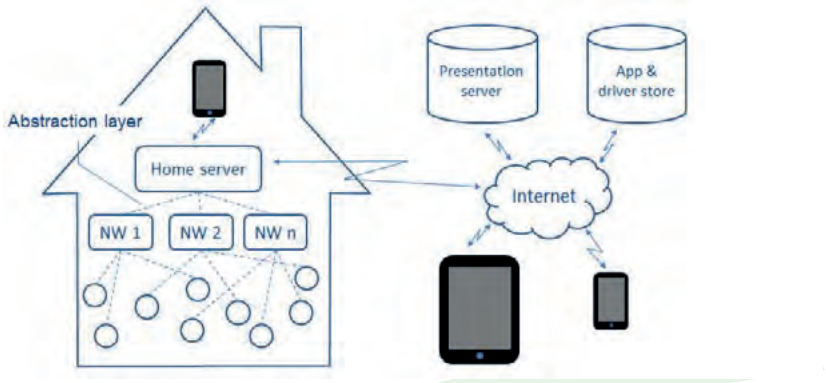
CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

CATRENE
Cluster for Application and Technology Research in Europe on NanoElectronics

CA103 | Energy-Efficient Home Networks [HERTZ]

Hertz
Energy Efficient Home Networks

Energy efficiency is high on the European agenda. However, even with the arrival of regulations to phase out incandescent lamps and the introduction of various forms of energy-efficient lighting, a significant amount of energy continues to be wasted in homes and offices. The main contributor to this situation is that lights or other appliances are often left on when they are not required. The CATRENE HERTZ project has taken the first steps towards the introduction of auto-adaptive networking devices that limit energy wastage in both domestic and commercial equipment, without human intervention.



Auto-adaptive consumer networks lead the way in energy saving

For many years, it was thought that the home automation market was on the verge of centralised control or networking of all electrical appliances, from the washing machine to the refrigerator to the television to lighting. It has long been acknowledged that true energy efficiency requires automatic control systems.

However, in order to help the expansion of the market for such consumer networks, the members of the HERTZ consortium identified key challenges that had to be confronted. Firstly, it was essential to analyse the power consumption of such a network and to demonstrate that the amount of energy saved was greater than the amount of energy needed to make the saving. The consortium then worked towards a solution that is easy to use and can be installed by an ordinary consumer without having to rely on a professional. Finally, they addressed the issue of compatibility between proprietary devices and the risk that their presence in isolated clusters would hinder market development. All of these challenges were examined by the consortium while, at the same time, aiming to minimise the cost for the consumer.

The results of the Hertz project have led to substantial progress in this domain (sometimes called the Internet of Things), with the establishment of a set of standards that will form the basis of a compatible home automation network of the future.

A comprehensive solution

Over the three-year duration of the project, the consortium members worked together to establish a scenario that will serve as the European basis for the future energy-efficient networking of home appliances. The goal was to provide the means of controlling the functionality of disparate devices in such a way that overall efficiency is substantially improved.

The first stage in this process was to address the use of lighting energy. A large step was already taken with the phasing out of low-efficiency incandescent light bulbs. The next step has to be the efficient use of the new low-energy light sources and especially solid-state lighting (SSL). In fact, the efficiency of SSL lighting is already so good that it's a challenge to see how existing wireless networks could be used to control lighting without wasting energy. This is very much the case with

Partners:

ADD Semiconductor (acquired by Atmel)
Dialog Semiconductor
DS2 (acquired by Marvell)
Infineon Research
Infineon Wireline Division (spun out as Lantiq)
Iquadrat
Philips Consumer Electronics (spun out as TPVision)
Philips Lighting
Philips Research
Quintor

Project leader:

Henk Schepers
Royal Philips Electronics

Key project dates:

Start: October 2009
End: September 2012

Countries involved:

Austria
Spain
The Netherlands

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	
Health and aging society	
Safety and security	✓
Energy efficiency	✓
Digital lifestyle	✓
Design technology	
Sensors and actuators	✓
Process development	
Manufacturing science	✓
More than Moore	
More Moore	
Technology node	45/32 nm

WiFi systems, which have been shown to waste 80% of the energy in protocol maintenance while only 20% is used for data transfer. Providing SSL users at home or in the office with more comfort and safety without wasting energy is not easy using existing WiFi protocols.

Consumer acceptance dictates 'no new wires'. Where possible the existing electrical infrastructure will be used to power a sensor or to exchange information between system components (power-line communication) but, preferably, wireless control and mains-free power is required. The challenge was, therefore, to first of all devise new wireless methods of connectivity that are substantially more energy-efficient. To enable battery-free operation and to avoid frequent battery replacements, a second challenge was to develop much more precise sensors. Furthermore, the accuracy of those sensors had to be improved to ensure consumer satisfaction.

Dedicated components

The HERTZ project has successfully addressed component-level technology concerns, by creating an energy-efficient true presence sensor, a fully-harvesting powered daylight sensor and a wireless clip-on power sensor allowing disaggregated power measurements.

To achieve much more energy-efficient wireless networking, the HERTZ project has brought about the development of:

- a bi-state receiver concept with a wake-up sensitivity of -90 dBm at only 5 μWatt
- an ultra-low energy (ULE) variant for DECT with a sleep-mode consumption of 3 μA instead of the continuous 2.2 mA for normal DECT and a burst-mode consumption of only 2 mC
- an energy-efficient wireless local area network (WLAN) stack that performs up to 90% more efficiently in specific use cases
- a power adjustment scheme for the ZigBee wireless specification that leads to a 27% reduction in consumption.

The HERTZ project has also defined a gateway interface specifically tailored to the integration of different network technologies. As the various HERTZ members are leaders in their respective fields, the expectation is that this interface will help to give a realistic boost to the development of the home energy-control market.

Finally, the introduction of a self-configuring application and driver store provides for simple plug-and-play system installation.

The basic infrastructure

As a result of the HERTZ project, the control and/or monitoring of energy consuming appliances, in the home or in a commercial environment, has become a reality. The true presence sensor provides the means of determining a human presence in a room, even if the subject is motionless. The HERTZ gateway offers a means of wirelessly interfacing to a wide range of other devices that can signal their status over the network. The network protocols developed in the HERTZ project set standards that appliance manufacturers can use to enable their products to communicate, eliminating the incompatibilities that restrict the average consumer.

Overall, the HERTZ project has created the basic infrastructure for a comprehensive network control system that will greatly improve the efficiency of energy consumption in homes and commercial premises. It is confidently expected that electrical appliance manufacturers will, in future, follow the trend of providing their products with external interfaces conforming to the standards developed in the HERTZ project.

Cluster for Application and Technology Research in Europe on NanoElectronics

CA301 | High Dynamic Range Low Noise CMOS imagers [HiDRaLoN]

The purpose of the CATRENE HiDRaLoN project was to address societal needs in such areas as healthcare, entertainment as well as road and industrial safety. The results are expected to provide greater efficiency and fewer errors in medical diagnostics; unprecedented TV image quality; automatic visualisation of road driving conditions; enhanced image quality in low-light conditions and improved safety on production assembly lines. The successful completion of the project has resulted in the availability of CMOS imagers that are set to replace the CCD imagers that have dominated the market for many years.

CMOS image sensors now set to replace CCD technology

During 2011, the project worked towards the availability of full complementary metal-oxide on silicon (CMOS) image sensor designs and started the development of the final demonstrators. In 2012, the silicon for full CMOS imager designs was available and was evaluated. The final demonstrators were completed and were used to show the improved functionality that has been secured.

Research topics included pixel design and modelling, low-noise analogue read-out, including analogue-digital (A/D) conversion and multiplexing, modelling of thermal, optical and electrical cross-talk, optics and correction algorithms for CMOS imager and optical enhancement. The HiDRaLoN project focused on increasing the dynamic range of CMOS imagers to 120dB and lowering the noise level by at least 50% to make CMOS imagers better than today's charge-coupled devices (CCDs). Currently, CCDs still hold a dominant position over CMOS image sensors at the higher end of the market.

Best practices from CCD manufacturing have been retained so it is expected that the CCD imagers currently used in high-end broadcast equipment will now also be replaced by HiDRaLoN CMOS imaging devices.

Functional prototypes of full imager chips for medical, broadcast, time-of-flight and machine vision were evaluated and achieved or exceeded expected results. Furthermore, all planned application demonstrators based on medical, broadcast and time-of-flight imagers were built and were fully functional.

Tests with a new industrial vision test chip proved the functionality of new building blocks and concepts and exceeded the expected results of required optical performance.

The project has delivered five new imagers for the general time-of-flight, medical, broadcast and safety/security/machine vision markets, as well as algorithms to correct flaws in the imagers and the optics. For broadcast purposes, two new lenses have been designed and evaluated together with correction algorithms designed within the project. Demonstrations in the project have focused on medical, broadcast and general three-dimensional (3D) applications.

All of the main objectives of the project were achieved and all deliverables were completed. Excellent co-operation between the partners resulted in continued co-operation even after the end of the project.

Partners:

Budapest University of Technology & Economics
CRS iiMotion
e2v Semiconductors
Fraunhofer Institute
Grass Valley
Helion Vision
IMS Chips
Le2i (University of Burgundy)
Nikhef
Philips
Pilz
Technical University of Delft
Thales
Deutsche Thomson OHG
Viimagic GmbH

Project leader:

Klaas Jan Damstra,
Grass Valley (NL)

Key project dates:

Start: March 2009
End: June 2012

Countries involved:

France
Germany
Hungary
Israel
The Netherlands

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	✓
Health and ageing society	✓
Safety and security	✓
Energy efficiency	✓
Digital lifestyle	✓
Design technology	✓
Sensors and actuators	✓
Process development	✓
Manufacturing science	✓
More than Moore	
More Moore	
Technology node	45/32 nm

Several fields of application

While the potential range of applications for HiDRaLoN CMOS sensors is extensive, the main markets explored were medical, broadcast and industrial.

The advances obtained in the medical domain primarily involve imaging enhancements in x-ray and computer tomography (CT) equipment. The sharper images that are now possible through HiDRaLoN CMOS image sensors, greatly improve the accuracy of diagnosis to the benefit of patients and medical staff.

For applications in the broadcast environment, the first full-sized CMOS image sensors were extensively evaluated within the HiDRaLoN project. At the end of 2010, it was decided that the performance of the prototype was already so good, that it could be used to start the development of new commercial products. While the research on the CMOS image sensor continued within HiDRaLoN, parallel development continued on the first two commercial products.

There is an increasing demand and awareness in industry regarding new high dynamic range (HDR) image sensors which drive new applications or enable new image processing based systems. In addition to market reports, this is also apparent in both industry oriented and scientific conference programmes dealing with the HDR topic.

In the industrial production line environment, HiDRaLoN project developments have opened doors to considerable opportunities:

- The industrial vision image sensor developed in the project is intended to be used in new safe camera systems developments for three-dimensional zone monitoring.
- Applications requiring HDR imagers, such as welding process monitor and control systems. The main added-value lies in the reduced cost of high-performance systems.
- IMS CHIPS will deliver qualified CMOS image sensors to industrial applications in Europe in volumes of up to several tens of thousands of units per year.

In addition to machine safeguarding and the machine safety market other markets with possible applications of the logarithmic industrial vision imager are:

- Intelligent video surveillance cameras
- Automotive safety systems
- Medical imaging

Significant project outcome

The HiDRaLoN project has made a substantial contribution to the advancement of European CMOS image sensor developments. The results will have far reaching consequences for the European silicon fabs as well as for end-users in several fields of application.

All of the main objectives of the project were achieved and all deliverables were completed. Excellent co-operation between the partners resulted in continued co-operation even after the end of the project, both commercially and in terms of new European projects.

The project resulted in a long list of publications and the filing of 6 patents.

A substantial contribution was made to the EMVA1288 standard for High Dynamic Range (HDR) sensors (in version 4.0 the standard will be extended to non-linear and HDR cameras) and a Time-of-Flight Study Group was inaugurated.

One of the key factors in all CATRENE projects is the creation of a consortium of expert partners who can work together to achieve results that will advance the European strengths in various aspects of advanced technology. The CA301 project has adequately demonstrated the value of that process and the results achieved serve to illustrate the benefits.

CATRENE Cluster for Application and Technology Research in Europe on NanoElectronics

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

PROJECT RESULTS

CA303 | Fault-mitigation electronics is the best defence against soft, firm and hard errors in critical applications [OPTIMISE]

Electronic systems deployed to control critical functions – such as in aerospace, avionics and automotive applications, as well as, in crypto-graphic chips, medical implants, networking and servers – need to be secured against errors in the information flow, and failures in electronic components. The OPTIMISE project developed optimised mitigations for advanced digital and power electronic systems that cope with the issue of reliability in the face of increasing soft, firm and hard errors.

Platforms, like satellites, launchers, aircrafts and cars, have electronic systems which are often subjected to harsh environments capable of inducing errors in their information flow, and failures in components. High-energy particles present in space, for example, cause errors and failures in space electronics. With the sharp increase in the use of computing, electronic systems, even on the ground, can be impacted. Both digital and power electronics are affected, and in the latter case, radiation can be destructive. For space, avionic or automotive applications, the mean requirement for safety critical functions is 1-10 failures in 109 hours. The answer is to develop optimised mitigations for these electronic systems in order to successfully improve reliability to counter the increasing problem of so-called soft, firm and hard errors.

Risks assessed and mitigation techniques optimised, validated and deployed

This project had three key aims:

1. To develop and validate mitigation techniques, from layout to application architecture levels, for three applications specified by different end users in automotive, avionics and space;

2. To acquire knowledge on new radiation threats that may impact future electronic equipment, and work in close collaboration with standardisation bodies to propose guidelines or standards to be able to perform relevant risk assessment;

3. To benefit from the synergies in the project to achieve one of the first detailed radiation risk assessments for automotive.

Validating mitigation techniques was conducted in two phases. Proof-of-concept mitigations were applied to simple test cases (such as simple test structures implemented on a test vehicle, power devices manufactured and the use of the well-known Leon soft processor) and the efficiency was then assessed based on experiments. Developed mitigations were then deployed (with some adaptation), where possible, in end-user applications, and their efficiency assessed.

Project results look promising. The proposed mitigation optimisation for the avionic system-on-chip (SoC) application passed assessment. The latest test vehicle embedding the mitigated version of the space ASIC (V53) was successfully produced in December 2013. The assembled and functionally tested parts were made available in May 2014, radiation tests and the exploitation of the results performed in June 2014, and a first assessment of the radiation risk for automotive done in 2013. In terms of product development, a new commercially available power diode (1200V SiC STPSC6H12), which offers better radiation tolerance, has been available since 2013.

In short, OPTIMISE resulted in a set of validated mitigation techniques (from layout to application-architecture levels), customised mitigations for given applications and a strong argument for standardising error assessment.

Close European working

Mitigation development was achieved through the close collaboration of some 20 Spanish and French project partners, ranging from semiconductor manufacturers and their technology developers, to academic partners and end-users.

It is worth noting OPTIMISE's close interaction with RELY, a complementary project. While both deal with improving system dependability, OPTIMISE's focus is in developing mitigations for radiation effects, whereas RELY's is in the design of reliable SoCs.

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Safety and security
- Energy efficiency
- More than Moore

PARTNERS

AIRBUS
ARQUIMEA
ATG
ATMEL
CEA, DAM, DIF
CNM
Continental
D+T Microeletronic.
EADS IW
IM2NP
IMS
iRoC
Renault
STM (Rousset)
STM (Tours)
TAS-E
TIMA
UC3M
UIB
VALEO

COUNTRIES INVOLVED

France
Spain

PROJECT LEADER

Florent Miller
Airbus

KEY PROJECT DATES

July 2009 - June 2013

All partners contributed to the dissemination effort, with presentations at six events and through more than 120 publications. Standardisation was also pursued through workshops to promote tools and test methodologies and update of avionic radiation test standards. In automotive, a standardised method for assessing reliability due to radiation effects on power components was proposed.

Impacting technology, business and safety

This project helps make possible the use of advanced electronics in critical end-user applications, and ensures the reliability of consumer electronics. Let us look at some market demands, business opportunities and benefits from which OPTIMISE's deliverables and other results can profit.

Electronics – sensors and intelligence – are found everywhere in cars, increasing safety through driver assistance and drive-by-wire systems. And the all-electric car will push the use of power electronics even further. Studies show that sales of electrical vehicles have already increased by 50% since 2012. This trend is expected to continue. Now, considering reliability of electronic components is an essential element in lots of applications (including automotive domain and more particularly, power electronic applications), the number of power components is also expected to increase significantly. Similarly, SmartPower-type devices which are used in many automotive power applications, also follow the same trend. Between 2005-2014, the number of SmartPower devices in a single product has increased by factor of four, and the number of products in production by about a factor of two.

A main challenge in the avionic sector is the ability to implement high performance ICs while ensuring the required safety level. OPTIMISE now offers solutions to support these and other avionics requirements. In space, satellites and launchers are totally autonomous so their reliability has to be determined prior to launch. In recent ESA space projects, complex digital and mixed signal functionalities require their integration into a single chip, making the chip size and power consumption critical for the development of the application. This also means that radiation-induced mitigation techniques, related to chip size and power consumption, also need to be optimised. Advances from OPTIMISE will allow the implementation in space chips of some functionalities that were not implementable using classical radiation mitigation techniques. Another key outcome of OPTIMISE is the development, assessment and validation of a complete 90nm digital rad-hard standard cell library.

Finally, regarding safety, OPTIMISE will provide competitive strength in sectors of European industry that need to make use of 'fail-safe' electronics in automotive, aeronautics and space applications, as well as, in those that provide enabling technology for low-power consumer electronics. At the same it will also ensure increased human safety.

CATRENE Office
9 Avenue René Coty
F-75014 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

Energy-efficient devices and energy control systems

Cluster for Application and Technology Research in Europe on NanoElectronics

CA501 | Low-power design approach launches new developer community

Communication-centric heterogeneous multi-core architectures (COMCAS)

Mobile communications are the most important consumer-electronics market worldwide. Yet as features and customer expectations grow, they run up against the same brick wall – battery life. Only by reducing power consumption can manufacturers introduce innovative new features. The challenge for COMCAS was to improve battery life significantly for small-form-factor devices by reducing power consumption. The CATRENE project developed new low-power approaches for semiconductor design which can reduce power consumption by a factor of five. The results are already being exploited in smartphones.

The global market for mobile devices is billions of units a year. Yet the early leadership Europe gained with the GSM mobile phone standard is under attack from Asia and its lower production costs. Innovation is considered key by European companies to maintaining market share; and for mobile devices, particularly smartphones, cutting power consumption is critical.

Such a reduction is crucial because, with a typical modern smartphone, watching a video exhausts the battery within two hours. Most consumer-electronics suppliers – as well as their customers – now consider minimum acceptable battery life between charges to be seven hours, or the length of a typical working day.

The CATRENE CA501 COMCAS project aimed to improve battery life for small-form-factor devices by focusing on low-power solutions for communication-centred multi-core chip architectures. It examined the complete low-power design hierarchy, including systems-level choices, modelling of applications – algorithms and protocols – and architectures, how to maximise reuse of existing intellectual property, partitioning and mapping, virtual prototyping and minimal-power design.

Reducing power use

COMCAS's goal was to reduce total power consumption by a factor of five while maintaining performance at current levels. It targeted 45 and 32 nm CMOS production technologies, building on the results of the MEDEA+ LoMoSA+ project which developed European low-power expertise in homogeneous architectures for mobile and multimedia. The key difference was its focus on communication-centred multi-processor architectures which require new architecture, circuit and software tools to engineer circuits with an unprecedented level of complexity.

The main design innovation was to move from a traditional performance-oriented approach to one in which performance and power consumption were considered in a more integrated manner.

Key elements were:

- Communication-centred run-time configurable heterogeneous multi-core hardware and software;
- Advanced power management at platform level;
- High-level power-estimating tools able to deliver an accuracy of within 20% of actual energy consumption; and

ENERGY-EFFICIENT DEVICES AND ENERGY CONTROL SYSTEMS

Partners:

ATRENTA
AXIOM-IC
CEA-LETI
CEA-LIST
CNRS [LEAT]
NXP Semiconductors
Recore Systems
STMicroelectronics
ST-Ericsson
Synopsys
Thales
TIMA
TUD

Project leader:

Armand Castillejo
ST-Ericsson

Key project dates:

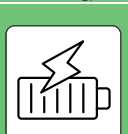
Start: March 2009
End: February 2012

Countries involved:

France
The Netherlands

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	✔
Design technology	✔
Sensors and actuators	
Process development	
Manufacturing science	✔
More than Moore	
More Moore	
Technology mode	45/32 nm



Energy-efficient devices and energy control systems

- Innovative electronic design automation flow and tools.

All these elements needed to be taken into account in an integrated manner if the project was to deliver a significant power reduction.

Underpinning a community

COMCAS met its targets, developing demonstrators for four application domains – video, radio, telecommunications and advanced techniques in 32 nm – confirming the advances achieved. Two demonstrators were shown at the 2011 Nanoelectronics Forum in Dublin, where COMCAS won the first place in exhibition awards. One showed the gains from a new high-performance dual-core processor. The second demonstrator of power characterisation for a programmable architecture resulted in a significant advance for H264 kernel processing using a coprocessor-based accelerator – also known as PraXia – involving a successful collaboration between partners Atrenta and CEA-LIST/CEA-LETI.

The dual-core chip has now been incorporated into a new kit for developers. Snowball is a low-cost, small-form-factor yet powerful mother board for fast development of mobile applications. It combines ST-Ericsson's Nova A9500 dual-core application processor with an innovative MEMS combining a 3D gyroscope, accelerometer, magnetometer and a barometer, GPS, WiFi and Bluetooth features, all in a small battery-operated device. With support for 3D graphics, high definition video and HDMI output, Snowball puts leading-edge video and mobile technologies within reach of a wider community of developers and hobbyists.

Launched at the Mobile World Congress in 2011, Snowball helps software developers to harness the capabilities of the most advanced smartphone and tablet platforms available. It is already leading developers to create applications for Android, Linaro, Meego and Ubuntu, and has given rise to its own open-source developer community, Igloo (**http://www.igloocommunity.org/**).

New market sectors

Partner NXP has been able to develop a near-field communication (NFC) capability for a one-chip design; reduced power consumption enables the chip to handle more NFC data than earlier versions. These capabilities endow chips with important additional features; an NFC-equipped smartphone can be used to pay fares on board buses or trams for example.

NXP also joined with another company in late 2011 to release a NFC-managed online game. Skylanders, already a great success in the USA, enables gamers to keep their own personalised character and environment on a small, easily portable NFC device, and to enter or leave an online game at any location simply by passing the device through the terminal field.

COMCAS also led to several the patents – NXP filed one patent and ST-Ericsson filed two – in particular on power-efficient branch predictions and improved scalar distribution in an SMID system – while UPV filed one on on-chip communication and LEAT filed one on multiprocessor low-power schedulers.

Overall the results will help consolidate Europe's position in the aggressive and fast-growing smartphone market while enabling companies here to attack new radio and video segments – particularly video surveillance.

Finally, the COMCAS results led to a proposed new CATRENE project, BENEFIC, to determine the best energy-efficient solutions for low-power design. BENEFIC is expected to maintain the effort on power reduction through energy harvesting.

CATRENE
Cluster for Application and Technology Research in Europe on NanoElectronics

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
Tel.: +33 1 40 64 45 60 - Fax: +33 1 43 21 44 71
Email: catrene@catrene.org
http://www.catrene.org

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CT105 | 3D-TSV integration improves multimedia and mobile device applications and helps industry [3DIM³]

Cramming more electronics onto a chip, could make consumer devices, like mobile phones and tablets, even more compact, run more functions and faster, use less power and even cost less. What makes all these benefits possible is 3D integration. The heart of the 3DIM³ project, this emerging technology can produce highly integrated systems by stacking them vertically (height being the third dimension, hence 3D) and connecting various materials, technologies and functional components together using a high-performance technique called TSV. This project brought together successfully European partners with specialised expertise and experience in the design and production of integrated circuits based on system-on-chip and system-in-package technologies.

Deploying the technique of 'stacking', three-dimensional (3D) integration is an attractive option for many advanced consumer products. It brings together different types of chips and devices in a single package or a compact subsystem, thus gaining maximum benefit from highly specialised and heterogeneous technologies.

By replacing single-chip packages with 3D devices, higher transistor density and power savings are achieved; distances are shortened for data to travel; and manufacturing costs reduced. Key to stacking is the use of 'through silicon via' (TSV) – a chip-assembly technique which impacts the overall electrical and physical design process. However, to take full advantage of 3D integration, the decision must be made early in the architecture planning process, rather than as a packaging decision after circuit design is complete.

This requires taking 3D design space into account from the start of system design in order to distribute the different components into a new set of chips that need to be stacked. However, prior to 3DIM³, there were several obstacles in the way of mass producing 3D integrated circuits. These hurdles ranged from the unavailability of proper CAD tools and a test methodology, to low manufacturing yields (thin-wafer handling process) and unacceptable reliability.

Essential ecosystem

That is where 3DIM³ comes into its own. This project created the ecosystem that is enabling European industrials to exploit 3D stacking capabilities, by delivering all the main building blocks to start the design of a full 3D integrated system:

- TSV & TEV models and design rules
- 3D design kit
- Pieces of design flow
- 3D interconnect and protocols
- 3D test procedures

Importantly, the four demonstrators validated the 3D-TSV design flow, tools, methods, and interconnects developed during the project.

Partner gains from co-operation

This project underscored the benefit of co-operation and confirmed what is technically and technologically achievable through such collaboration. Crucially, it switched the mind-sets of project participants to think '3D', and to start designing and verifying, complete systems with new architecture paradigms regarding standards evolution, testability, design methodologies and heterogeneous components.

Furthermore, all 14 project partners also confirmed direct benefits to their own business, or institutional activities in the case of universities. Benefits included access to advanced technology, methodologies for 3D-IC design flow and 3D-TSV tools (designing 3D circuits, for example), and the issuance of related patents.

Key partnerships were formed to establish ways of implementing the 3D chip, and to extend a leadership position in EDA methodology and tools for 3D-TSV technology.

There was also an increased understanding of TSV technology and performance, especially in RF applications; and on the process of the integration of heterogeneous technologies and to find a mixed integration solution for silicon and dies.

ENERGY-EFFICIENT DEVICES AND ENERGY CONTROL SYSTEMS

Partners:

Cadence Design Systems
CEA-LETI
EADS DS
Fraunhofer Institute
Infineon Technologies
Lyon Institute of Nanotechnology
NXP Semiconductors
R3Logic
Recore Systems
STMicroelectronics
TIMA Laboratory
TU Delft
University of Erlangen-Nürnberg
Virage Logic

Project leader:

Dominique Marron
STMicroelectronics

Key project dates:

Start: July 2009
End: December 2012

Countries involved:

France
Germany
The Netherlands

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	
Digital lifestyle	
Design technology	✓
Sensors and actuators	
Process development	✓
Manufacturing science	✓
More than Moore	✓
More Moore	
Technology node	

And with unique expertise comes competitive advantage. The acquisition of significant knowledge and understanding in the interconnectivity between the specific analogue device and the high speed processing component (decoder) strengthened one electronics company's leadership position in the home gateway market.

Academic institutions participating in 3DIM³ also profited from a tight collaboration with industrial partners, and from technological advances and know-how in new packaging technologies. They were also able to set up a framework to promote future 3D research initiatives, and consolidate their leading academic position in Europe on computer architecture and embedded systems.

Maintains competitive edge

For consumers and end-users, as mentioned earlier, 3DIM³ means even smaller, faster, cheaper mobile phones and tablets that contain more functions and consume less power.

But what is the impact of 3DIM³ on the industry as a whole?

Innovative 3D design solutions will enable European multimedia, mobile device manufacturers to increase the ability of their designers to build larger and better quality systems in less time and at lower costs. This means that these device manufacturers will be able to maintain leadership in this strategic market.

The know-how improvement in 3D integration will also impact semiconductor fabs (fabrication plants) by improving the production process in the near future. Critically, this project's contribution to the European knowledge will secure Europe's future forefront position in semiconductors worldwide.

The increased production of 3D devices and increasing complexity of managing the 3D products will drive widespread adoption of 3D design for mobile and multimedia devices.

Of course, it will take some time before 3D products can be massed produced, but the work and results from 3DIM³ can already be used to define the architecture of highly complex products, thanks to the technological achievement this project produced in modelling, architecture, algorithms and CAD.

Most encouragingly, the design experience of 3DIM³ continues to be felt through seminars and workshops, targeting European designers, with the objective of improving on the design experience 3DIM³ started.

And the fact that universities are now adding 3D system design to their curriculum further confirms that 3D stacking is here to stay.

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

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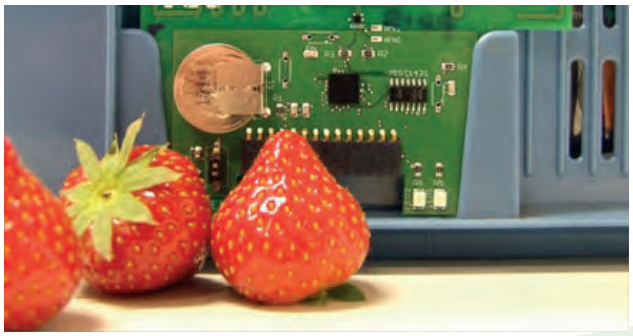
Cluster for Application and Technology Research in Europe on NanoElectronics

CT204 | Using smart electronics (RFID) to monitor quality of perishables (PASTEUR)

PASTEUR touches our daily lives. In helping to ensure perishables arrive at their destination in good condition, this project reduces the amount of damaged food and spoilage – an annual loss of €25 billion to the food industry and €300 to every household. Deploying sensors based on Radio-Frequency Identification (RFID) technology, PASTEUR has developed a wireless sensor platform that is able to monitor a far-wider range of environmental parameters than was previously possible, and extend environmental monitoring to crates and boxes of perishable goods along the logistics supply chain.



Central to this solution is the wireless sensor tag, based on a multi-sensor chip that connects to an RFID chip and a low-power microcontroller. This combination of technologies enables autonomous logging of the environmental conditions of products during transport and storage in the cold chain. RFID-based environment monitoring is a technology with the potential to transform the present-day supply and distribution chain. On the one hand, it will improve cold-chain distribution quality and record-keeping; on the other, it will also assist in identifying problems, assigning liability, and ensuring timely preventive measures are taken.

Successful delivery of key technologies

The main project deliverables are several important technologies (power, sensors, wireless communication and security) key to the sensor tag and related equipment, and which were developed and integrated in a single unit. These were tested – with the help of 'demonstrators' – for integration, cost-efficiency and application relevance.

PASTEUR deals with quality monitoring of food products in two main application areas:

1. Fruit: cold chain monitoring (logging of temperature and different gas fractions);
2. Meat: monitoring temperature and pH (acidity or alkalinity) value after slaughtering.

Considering that these measurement systems differ widely by their very nature (measuring in gas is quite different from measuring in liquid), it was logical to define and develop two separate demonstrators:

1. An integrated smart sensor tag (with temperature, humidity and possibly CO_2 sensor capability) for fruit (explained above);
2. An integrated smart pH sensor package (with temperature and pH sensor functionality) for meat.

The pH sensor consist of two components: a moulded stick (containing the sensitive pH sensor device), which is connected to a small custom printed circuit board which contains an ARM microcontroller, a battery and several other auxiliary components, including a connector for serial communication and a connector for a (optional) external reference electrode.

All deliverables successfully were tested and verified in field trials comprising a simulated cold chain, and a carcass in a slaughter house. There were also encouraging technical achievements in the deployment of active RFID labels in cold chain monitoring. Energy consumption was reduced to a low 0.5 mA (current). The tag size was kept to a compact 10 cm^2 and all functionality integrated in a single interface between printed and silicon element for both types of tags. In addition, a low tag price (of just over US$ 1.00) was achieved.

ENERGY-EFFICIENT DEVICES AND ENERGY CONTROL SYSTEMS

Partners:
Boschman Technologies
Centro Nacional de Microelectronica (CNM)
IMEC-NL
Inkoa Sistemas
KU Leuven
Netherlands Packaging Centre (NVC)
NXP Semiconductors
Philips Consumer Lifestyle
Philips Innovation Services
Philips Research
Prelonic Technologies
Royal DSM
Stichting IMEC-NL/Holst Centre
TNO/Holst Centre
TP Vision
TU Delft
TU Eindhoven
Verhaert New Products Services
Wageningen UR

Project leader:
Romano Hoofman
NXP

Key project dates:
Start: July 2009
End: September 2012

Countries involved:
Austria
Belgium
The Netherlands
Spain

PROJECT CONTRIBUTES TO

Communication	
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	
Digital lifestyle	
Design technology	✓
Sensors and actuators	✓
Process development	
Manufacturing science	✓
More than Moore	✓
More Moore	

Benefits all around

Typically, around 20% of temperature-sensitive healthcare products are wasted during transportation due to a broken cold chain. Each year, suppliers of perishables ship over five billion pallets valued at $2.6 trillion of chilled meats, seafood, cheese, and produce, as well as temperature-sensitive pharmaceutical and biomed products.

This means everyone in the supply chain of any transported goods will benefit from PASTEUR's technology solution: from manufacturer to transporter to retailer, and finally end-user. In the future, retailers could use this technology to install a shelf-based quality control system at sales outlets, and consumers to check (through their mobile phone) the quality of their food at home. And reduced spoilage is also good for the environment.

European co-operation and collaboration

Key to the success of this project was the pooling together of European expertise and experience, combined with good management and communications. Crucially, the various project participants and partners contributed essential components and know-how on the different technologies in the 'value chain' of RFID-based intelligent sensor systems. Notable examples of this type of co-operation include FlexSMELL, a European project deploying RFID technology in developing an olfaction system; and Devlab in the Netherlands where wireless sensor networks are developed.

Future co-operation is also on the cards. The European project Chill-On, whose development work – combining TTI and RFID to locate and trace any food product – is of interest to PASTEUR's own R&D. Chill-On is also developing an Information Management System, similar to PASTEUR's own model, to control the parameters throughout the food supply chain. And Belgium's Flemish Institute for Logistics is also interested in collaborating in a national project.

Going forward

The real attraction of the PASTEUR solution is its use of smart sensor tags in environment condition monitoring, combined with integrating multiple sensors and applying this technology solution in multi-item management, followed by item-level tagging and monitoring.

Competitive solutions in this fragmented market either offer temperature-monitoring only, or are extremely expensive and bulky, serving high-end markets (such as pharmaceuticals) or logistic bulk management (such as large shipments).

PASTEUR therefore has a competitive price-performance edge. However, it has to move fast if it hopes to get a slice of this potentially huge pie: potential competitors, who currently do not provide sensors, only wireless ICs, are quickly moving in.

One way is to approach companies are already showing interest in using the PASTEUR solution in the environmental monitoring of their supply chains. Another is to involve insurance companies, already in the logistics chain, in the smart monitoring process. Some large forwarders are already working with insurance companies to implement monitoring systems in containers. By continuously monitoring a shipment, insurers can identify the time and probable cause of damage, and, importantly, the party liable. This could even promote and facilitate the introduction of PASTEUR's technologies in cold chain management by providing a clear picture of cost and performance benefits.

The application areas for technologies developed in the PASTEUR project are not limited to the monitoring of cold chains for perishable goods. The potential variety of applications from the successful development of marketable platforms are actually quite vast. They include for example: supply chain uses such as traceability and quality management; domestic applications like detecting hazardous gases such as carbon monoxide; as well as medical monitoring to ensure therapy compliance; and corrosion monitoring for the construction industry.

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CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

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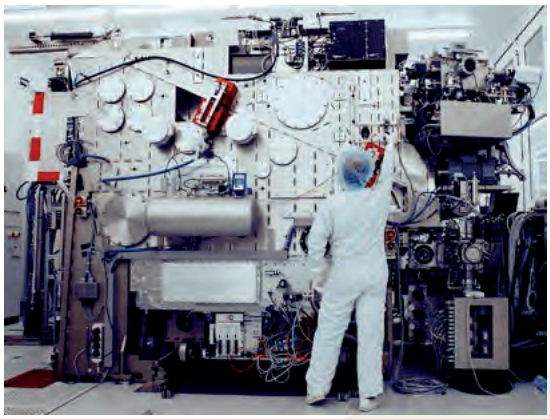
CT301 | Extreme UV lithography entry point technology development [EXEPT]

EXEPT

The extreme ultra-violet (EUV) lithography process is rapidly progressing as a viable production technique for less than 32nm semiconductor wafer technology. The CATRENE EXEPT project was set up to explore the possibilities for extending the lithography process to the 22, 16 and even 11nm nodes. The successful completion of the project now puts the European semiconductor lithography industry at the forefront of chip production expertise worldwide. During the course of the project, technology was developed to enable 22nm imaging at an acceptable cost-of-ownership in high-volume industrial-scale production.



Extreme ultra-violet lithography comes of age

Over recent years, EUV lithography has gradually become the standard process used for volume semiconductor manufacturing. Through the use of double patterning technologies, it has been possible to extend the application of immersion lithography to the 32nm node. However, EUV is capable of far higher feature density and therefore allows for a greater level of functionality in a standard chip package. Consequently, the primary aim of the CATRENE EXEPT project was to develop the necessary technologies, tools and infrastructure components as required for high-volume EUV lithography for the 22 nm node while laying the groundwork for extension to 16nm and 11nm nodes.

The CATRENE EXEPT project brought together a consortium of fifteen of the leading players in the European semiconductor equipment manufacturing industry and institutes with the aim of comprehensively extending the lithography tool technology to enable imaging at the 22 nm node at an acceptable cost of ownership level for industrial chip production as well as to develop EUVL infrastructure components for which competence and an industrial base exist in Europe. With the introduction of EUV lithography for high volume semiconductor production lines, the project aims at opening new business opportunities for the participating companies, at positioning the institutes at prominent international levels in their fields of activities and overall at safeguarding the international semiconductor industry in enabling the realization of the technology roadmap in lithography as given in the ITRS. Significant progress was already achieved on the 32nm platform in 2011 and this progress continued in 2012. Several 32nm pre-production tools are now operational at customer sites running wafers for process development. Tools were shipped employing both the laser-produced plasma (LPP) source and the discharge-produced plasma (DPP) source. Work on source debris mitigation and a collector prototype, ready for source collector module (SoCoMo) integration, has continued further outside the scope of EXEPT. This required an extension to the project in order to balance the various contributions.

Lithography at 22nm a reality

Development of the EUV lithographic platform for high-volume manufacture (HVM) at 22nm was progressively pursued throughout the course of the 3-year project. The system performance qualification of the 22nm lithographic tool started in the 2nd half of 2011 and continued in 2012. The final

Partners:

adixen Vacuum Products
AMTC
ASML Netherlands B.V.
Bruker Advanced Supercon GmbH
Carl Zeiss SMT GmbH
Dynamic Micro Systems Semiconductor Equipment GmbH
FOM institute DIFFER
Fraunhofer Institute for Integrated Systems and Device Technology (IISB)
IMEC - Interuniversitair Micro-Electronica Centrum vzw
IMS Chips
Media Lario Technologies
SAGEM Défense Sécurité
SUSS MicroTec Photomask Equipment GmbH & Co.KG
Xenocs
XTREME technologies GmbH

Project leader:

Gerold Alberga
ASML Netherlands B.V.

Key project dates:

Start: March 2009
End: June 2012

Countries involved:

Belgium
France
Germany
Italy
The Netherlands

PROJECT CONTRIBUTES TO

Communication	
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	
Digital lifestyle	
Design technology	✓
Sensors and actuators	
Process development	✓
Manufacturing science	✓
More than Moore	✓
More Moore	✓
Technology node	22nm

milestone was achieved in August 2012. The optics for the 22nm tool are based on the development of a high numerical aperture EUV lens and the irradiation lossless illumination system, with a high degree of illumination setting flexibility. This sets new standards of excellence in the field of semiconductor lithography.

Good progress was also achieved on the development of the source collector module. Due to the huge challenges involved in developing a production-ready system of this kind, the partners also collaborated in key technology areas outside of EXEPT to ensure that the relevant enabling technologies would be available when they are needed. One example is the EUV source technology, which has to be capable of more than 100 wafers-per-hour throughput.

The highly modular EUV lithographic system will allow for future upgrades and facilitates the distribution of the development work along the supply chain. Further EUV lithographic infrastructure components are developed. Those services include mask (repair and cleaning) technology and critical dimension (CD) metrology and should be seen as part of the whole EUV infrastructure.

The EXEPT project is a direct follow up to the EAGLE project (completed mid-2009), in which technologies for the EUV lithographic pre-production tool platform were developed. The EXEPT project enhances the prospect that Europe will further secure its world-wide leadership in the EUV lithography market. The project consortium members are companies from the European semiconductor equipment industry, several research institutes and a mask shop.

Most consortium members received funding from their respective national governments.

Ahead of Asian competitors

Over the last few years, there has been a growing interest in EUV lithography from the integrated circuit (IC) industry. This has been demonstrated during several conferences and in scientific publications at such events as the SPIE conferences, the EUV symposia and in several leading technical periodicals.

ASML, one of the consortium members, has already shipped six pre-production tool systems, (partly based on the technology developed in the earlier EAGLE project, with imaging capability close to 20nm) and has received 10 orders for the next generation, (the technology for which was partly developed in the EXEPT project). The shipment of the first of these new tools was made before the end of 2012. At that moment, the far-eastern competitors had not yet announced the shipment of any EUV tools.

With the completion of the project, the 22nm system is forecasted to become the first choice high-volume EUV manufacturing tool.

Potential for further development

The work performed in the EXEPT project, as a continuation of the activities of the earlier EAGLE project, has further matured both the EUV lithography technology and the EUV infrastructure. The results of the EXEPT project have contributed to an increase of employment opportunities in the EUV ecosystem and have provided the European semiconductor manufacturing industry with a leading position in the field of EUV lithography.

The successful development of EUV technology for high volume semiconductor manufacturing has exhibited the potential to provide new fields of European expertise for application areas that will emerge in the near future. These include lithography at wavelengths well beyond those covered in this project, biomedical microscopy, metrology, the development of elemental analysis equipment and advanced research on solar energy.

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9 Avenue René Coty - F-75014 Paris - France
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Cluster for Application and Technology Research in Europe on NanoElectronics

CT302 | Towards one European test solution [TOETS]

As semiconductor chip packages become more and more complex, the process of testing gains greater significance at all stages of manufacture and throughout the lifetime of the product. The CATRENE TOETS project was therefore established to investigate ways of unifying test procedures both within and outside the chip circuitry and is largely based on the concepts of built-in self-test (BIST) and built-out self-test (BOST). The project consortium assembled includes several of the leading European semiconductor manufacturers and integrators as well as research institutions supporting the industry.

A testing dilemma

The TOETS project was set up with the aim of creating a breakthrough in methods and procedures employed to test system-on-chip (SoC) and system-in-package (SiP) devices by treating the process of testing as an integral part of the whole value chain from design to application. To achieve this ambition it was essential to:

1. Supply test services to the final integrator and the end-user that would be valid throughout the lifetime of the product,
2. Develop chip design methodologies that provide enhanced matching of functional and test requirements, enabling a reduction in the cost of testing and achieving improved test efficiency through BIST and BOST solutions and the better use of test resources,
3. Acquire relevant information about the components at transistor level to adjust performance and improve product quality.

The major goals of TOETS, that needed to be achieved by the end of the project, were targeted at improvements in dependability in application areas such as automotive and healthcare where operational integrity is essential; reducing test costs or at least stabilising the cost of testing compared to the overall cost of integrated circuit (IC) development & production and shortening test development lead times (total time to market - TTM)

Lower costs, higher reliability

Another aspect of the project was to improve system integrity by embedding self-repair and self-calibration features within the chip technology. Methods were developed to diagnose system issues as well as provide solutions that would compensate for faults and restore system functionality in the event of component failure. In this respect, the consortium partners also worked on different heterogeneous systems (medical, automotive, etc.) but with the same objective of reducing system test costs and improving overall system reliability.

Devices used by consortium partners to demonstrate their solutions included:

- Low cost self-test and self-calibration sensors (micro-electro-mechanical (MEM), magnetic, capacitor, temperature, etc.) embedded in a system to ensure system integrity and the highest accuracy.
- An accurate self-calibration unit for level switchers used in the functional electrical stimulation (FES) context, to guarantee optimal communication between an implant and human tissue during the entire product life.

Developments achieved demonstrate the feasibility of system-level inbuilt calibration and self-repair. An overall improvement in product quality has been shown on several systems, including those involving sensor applications. Moreover, a reduction in the cost of testing has been achieved at system level as a result of the integration of the new embedded calibration techniques.

Reducing the cost of testing

Managing the cost of test (CoT) compared to the overall cost of chip manufacturing (CoGS, cost of goods sold) is the key to success in the very competitive semiconductor market. Consequently, the focus of the TOETS project was to develop testing

MANUFACTURING SCIENCE

Partners:

ATMEL
CEA-LETI
CEA-LIST
CNM-IMSE
D4T
e2v
INESC Porto
JTAG
KU Leuven
LIRMM
NXP Semiconductors
Ophtimalia
Q-Star
Salland
STMicroelectronics
ST-Ericsson
Supelec
Temento
TIMA
Tomorrow Options
University of Twente

Project leader:

Kees Veelenturf
NXP Semiconductors

Key project dates:

Start: March 2009
End: February 2012

Countries involved:

Austria
Belgium
France
Portugal
Spain
The Netherlands

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	✓
Health and aging society	✓
Safety and security	
Energy efficiency	✓
Digital lifestyle	
Design technology	✓
Sensors and actuators	
Process development	
Manufacturing science	✓
More than Moore	✓
More Moore	
Technology node	

methods that would contribute to cost reduction while at the same time increasing reliability.

The new device test architectures and alternative innovative test methods developed in the TOETS project provide new low-cost test solutions that allow the industrial partners to reduce their test cost, despite having only digital test equipment and by reducing test execution time per piece through higher parallelism of chip testing, even on high voltage ranges. Quantifiable and promising results have already been achieved by optimising the ratio of CoT/CoGS. Even so, there is evidently a demand for test equipment to cover the whole range of analogue and mixed signal (AMS) systems.

Currently, the only test programme generation tools available on the market are limited to purely digital test applications. None of the commercial (mostly US-based), tool vendors address the generation of analogue and mixed-signal test programmes. There are also no signs of test tool and electronic design automation (EDA) vendors indicating development plans for AMS test programme development tools. The concepts and prototypes for AMS test simulation based on defect simulation methodology, AMS/RF test programme synthesis and generation, developed in the TOETS project, will give the partners an advantage over the competition by reducing their test development time.

The computer test techniques toolbox based on statistical approaches and tools for BIST circuit evaluation will also give the partners an edge in test cost competition reducing test time and allowing low cost digital tester resources use.

Enhanced safety and reliability

Overall, it can be seen that the extent of the work performed within the TOETS project has covered a very broad range of component and application areas. Specialist applications, like those used in the aviation and automotive fields, will benefit from the enhanced safety and dependency resulting from the work done during the project. Medical uses of implanted FES devices will also directly benefit from TOETS project developments that considerably enhance reliability and precision. The development of BIST and BOST techniques, together with in-built automated repair, are advances that evidently greatly increase the lifespan of components and the equipment that they support.

By working together as part of the TOETS consortium, the various partners have shared knowledge that has enabled each of them to strengthen their individual role on the world stage and, at the same time, to enhance the position of the European semiconductor industry in the highly competitive world market.

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

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CALL 2

Cluster for Application and Technology Research in Europe on NanoElectronics

CA104 | Regular array of processors boosts performance and reduces design times and costs significantly [COBRA]

Process variability, lack of flexibility, excessive design-cycle times and unacceptable costs were key issues impacting conventional hardwired-based system-on-chip architectures, and which triggered the COBRA project. Its objectives were to develop and experiment with an open, flexible and high-performance platform deploying a regular array of processors, and driven by automotive, radio and video benchmark applications.

At the time, excessive design cycle times – close to two years – and relatively high costs were constraining hardwired system-on-chip (SoC) architectures and their effect on marketing potential. Furthermore, process variability was not yet well addressed for 32nm nodes and smaller. At the same time, however, massively parallel processor arrays were being used in high-performance embedded systems, and for hardware acceleration in desktop computer and server applications, such as video compression, image processing, medical imaging, network processing, software-defined radio and other computer-intensive streaming media applications.

Wide-ranging applications

With this in mind, the COBRA project was launched to define, design, assemble, and test an open, flexible, high-performance platform, based on a regular array of processors. Homogeneity was guaranteed by the architecture and by the use of a single type of processor, in contrast to heterogeneous hardware/software solutions. COBRA's main objective was to reduce the time and cost of the SoC design phase and thus provide European manufacturers with a strategic advantage.

The main result was a processing array hardware accelerator in 28nm CMOS technology that combines flexibility and performance, and which comprises four clusters comprising 17 processors. Hardware elements in this 'computing fabric' are connected through a network-on-chip (NoC) device and linked to the SoC host subsystem, together with 3D- graphics-rendering support hardware, data and instruction caches, interfaces to cameras and liquid crystal displays. This multimedia-oriented demonstrator is capable of running telecommunications, video and multimedia benchmark applications. Other COBRA techniques were demonstrated on mobile telephony (such as LTE receiver/transmitter) or automotive applications (like pedestrian detection).

Tool-kit eases and accelerates parallel programming

The COBRA platform also resolved other issues. It can control and fine-tune energy-consumption and – for a given application – help achieve an optimal power-performance trade-off. It allows for easy prototyping, especially with embedded software development: development time and effort to build and program parallel-processed applications are reduced through the use of three very fast simulation/emulation platforms – TLM, RTL and FPGA. These platforms also allow various architectural choices to be configured, tested and experimented with, largely made possible through the use of inter-processor communication that drastically increased performance.

Application-development time was further decreased through a tool-kit which assisted firmware developers to deal with inherent complexities of parallel programming. This tool-kit makes possible generating, debugging and mapping tasks to be carried out on available computing resources.

Complementary European partners

The project consortium involved two major European chipmakers and their partners. Usefully, one project member provided chips for a wide spectrum of digital consumer applications. Consequently, COBRA can considerably reduce

Partners:

ACE
CAPS Enterprise
CEA-LETI
CEA-LIST
Compaan
Ecomunicat
NXP Semiconductors
Sapec
ST-Ericsson
STMicroelectronics
Synopsys
Technical Uni Delft
Technical Uni Eindhoven
Tedesys Global
Universitat Autònoma de Barcelona
Uni Cantabria
Vista Silicon

Project leaders:

Philippe Garcin
STMicroelectronics

Kees van Berkel
Ericsson

Key project dates:

Start: January 2010
End: April 2013

Countries involved:

France
The Netherlands
Spain

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	✓
Health and aging society	
Safety and security	
Energy efficiency	✓
Digital lifestyle	✓
Design technology	✓
Sensors and actuators	
Process development	
Manufacturing science	
More than Moore	
More Moore	✓
Technology node	

time-to-market in these fields through its new methodology for rapidly assembling various product classes (including mobile phones and automotive) at different cost levels.

Integrating a hierarchy of computing resources with a set of embedded software and run-time functions was successfully performed by COBRA's project partners (thanks to their expertise in hardware, software and automation) who were able to implement hardware and software project elements efficiently and effectively.

Many partners – if not all – provided improvements to performance, through various techniques, such as optimising compilers (for execution speed) and memory bandwidth. And all COBRA partners were strong in design. Some of them offered innovative design techniques for parallel computing (technology push); others were familiar with the circuit constraints to be met in order to be attractive to the market (application pull).

Evolutionary high-performance platform

The soundness of COBRA architecture was fully proven, thanks to its one-die demonstrator fully functional on silicon. Power management was more advanced in COBRA than in competitor platforms, and its communication performance is comparable to its main competitors' offerings. Importantly, COBRA's development work was based on standards – some computing-oriented (such as OpenMP and OpenCL) and others application-oriented (like OpenCV and OpenLANp) – thus ensuring easy interoperability and IP-reuse.

Sharing project knowledge and experience worked well. There were more than 100 publications and conference presentations, and 10 new courses on offer are based on the work and achievements of COBRA. Six patent applications were also submitted.

Good market and business prospects

The global market for video analytics solutions is expected to pass the two billion dollar mark during 2014-2015. The forecast is that the smartphone market will evolve from US$ 481m in 2011 to US$ 927m in 2015, representing a CAGR of 18%. And the market in automotive electronic systems should reach US$ 249 billion in 2015, representing a yearly increase of 9.4% from 2010 to 2015.

COBRA is expected to contribute significantly to the potential of its partners to compete in worldwide markets, and it will secure the competitive power of several European industry sectors, such as telecommunications, TV, multimedia and high-performance computing. Architects and designers (hardware and software) at several project partners are already making direct use of project results.

Finally, there is the question of employment and other opportunities. COBRA will create jobs for small and medium-sized enterprises (SMEs) by providing access to high-technology achievements of larger companies. It will also help underpin the next generation of internal product-development for participating SMEs. Furthermore, this project will safeguard highly qualified jobs in the European nanoelectronics industry, including research centres. These jobs are expected to be inherently more sustainable in the face of Chinese and other Asian competition, thanks to the advanced technology and intellectual property at the core of products developed from COBRA's achievements. And by significantly increasing the degree of innovation present in future products, COBRA will in turn increase the size and utility of product portfolios of industrial partners, and thus help preserve and create jobs.

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CA202 | Radical 'what you touch is yours' authentication method for digital interaction [eGo]

eGo™

The eGo project provides an innovative way for users to interact wirelessly in a secure (ensuring privacy) and seamless fashion in the emerging world of the internet of things, and more generally to manage their digital interactions in an increasingly connected world. The eGo concept is based on the most natural and intuitive interaction humans can have with objects: through touch.

This project has successfully defined, designed, developed and tested a technology that establishes secure, bidirectional wireless channels between objects or individuals in the future internet of things (IoT), based on a bootstrapping scheme using the electrical conductivity of human skin. Notably, this so-called eGo technology opens the door to new and intuitive ways of interacting digitally.

By simply touching an eGo-compliant object with any part of your body, you in fact initiate a wireless 'pairing' between that object and the eGo 'controller' using body-coupling communication technology. The highly secure eGo device you wear can come in any form factor (like a watch, belt, jewelry or badge). All it needs is to be in close proximity to your body, without the need for direct skin contact. This intuitive way of wireless pairing drastically simplifies the design of man-machine user interfaces and the interactions with smart objects. Computing is no longer just what you see or what you hear. Another human sense comes into play: touch!

An important part of the project was the development of promotional and awareness tools, such as use-case devices and services, to demonstrate eGo's capabilities to the market in general, and several industries and application areas, in particular.

Ready to go

eGo technology has been successfully demonstrated in four different application domains – automotive, payment, access control and healthcare – and two reference designs (hardware and software) have been completed with a total software-development environment. In fact, eGo devices are in their final stage of fulfilling requirements for delivery, as the following results and achievements attest to:

- One month of autonomy (25 μA active sniffing mode);
- 150 ms transaction time capability for supporting highly constrained use cases (like door opening);
- Mass production UWB technology combining highly accurate, real-time localisation performances (±10 cm) with high data-rate communication (up to 6.8 Mb/s);
- 9D IMU integration (gesture recognition, fall-free detections, UWB and IMU fusion sensors);
- Integration in a watch (5 mm thick) and a volume (battery included) of 3000 mm3;
- Privacy retention through design support (for example, anonymous, authentic and non-traceable transactions);
- Water-resistance (no connector, no button, no holes);
- Adherence to Wireless Power Consortium's energy-interface standards;
- Fingerprint-sensor support;
- Ultra-thin and ultra-low power graphical display.

Award-winning success

This was a European collaboration undertaken by 12

ENERGY-EFFICIENT DEVICES AND ENERGY CONTROL SYSTEMS

Partners:

Worldline
CIT - Cork Institute of Technology
Continental
Decawave
Gemalto
IDEX
INRIA
Lincor Solutions
Precise Biometrics
STMicroelectronics (Tours and Rousset)
Tyndall Institute

Project leader:

Jean-Pierre Tual
Gemalto

Key project dates:

Start: July 2010
End: December 2013

Countries involved:

France
Ireland
Norway
Sweden

Project website:

http://www.ego-project.eu/

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	✓
Health and aging society	✓
Safety and security	✓
Energy efficiency	✓
Digital lifestyle	✓
Design technology	✓
Sensors and actuators	✓
Process development	✓
Manufacturing science	
More than Moore	✓
More Moore	
Technology node	

enthusiastic partners from France, Ireland, Sweden and Norway, who jointly created a large portfolio of advanced-technology components. Offering a vast range of new and intuitive possibilities needed to successfully address the emerging markets of internet of things and wearable devices, this eGo technology makes user interfaces and applications as simple as possible. For example, it can be prototyped and integrated in several form factors in miniaturised systems for new sensors, batteries and ultra-low power transmitters for body-coupling communication (via a natural connector: human skin).

Strong authentication, anonymity and non-traceability protocols were developed and implemented in the project, making the eGo concept both secure and privacy-preserving for managing digital interactions in the new IoT world. In addition, eGo integrated a highly secure microcontroller (comparable to ones embedded in smart cards) and ultra-wide-band wireless transmitters for communication and localisation. Prototypes of wearable devices incorporating the various versions of eGo proof-of-concepts with the key electronic system on chip (SoC) developed in the project – UWB and BCC controllers and protocol processor – were created and evaluated.

Demonstrators for four application domains – payments, automotive, access-control and healthcare – validated key eGo system characteristics. From these demonstrators, implementation guidelines and reference implementations, useful for further market developments, can be derived and wearable devices evaluated.

There were also achievements on the intellectual property front. Twenty patents were submitted, paving the way for the project standardisation strategy, which has entered a new phase as contributions specific to the eGo technology (UWB MAC/LINK layers) are ready for submission to the standards body, ETSI. This should provide European industry with a strong basis for entering the emerging IoT and wearable device market.

The eGo project was presented some 15 times at conferences and exhibitions, and cited or referred to more than 100 times by the international press. Notably, several project deliverables are ready for full commercialisation, including: DecaWave UWB SoC, the latest chip from the STM32 family; and a new patent-protected Idex fingerprint sensor. One of the project partners is also in contact with financial and telecom operators to launch some 'pre-series' to test market acceptance of the eGo technology; while two others are also looking into payments and retail opportunities. And a fourth is ready to provide a reference implementation to the Irish small- and medium-sized enterprise community.

And the list of accomplishments continues. In addition to awards in 2011 and 2012, the eGo payment demonstrator received the 2013 Innovative Payments Trophy for e-commerce products category at the Pay-Forum fair in Paris. In addition, the DecaWave UWB chip was nominated for 100 Hot products (Wireless category) for 2014 by EDN, and got the ICS New Product Innovation Leadership Award 2014 from Frost & Sullivan.

On the move

eGo technology and products will continue to evolve and grow in four ways, notably by:

1. Improving facilities at the server level for easing management and automated certification of applications and their secure synchronization between all eGo wearable devices owned by the user;
2. Improving the secure body-area network (for eHealth environments) and adding new sensors;
3. Sharing technology with partners and standardising air-to-air interfaces;
4. Introducing a secure, open and multi-application platform supporting trusted service management and full remote personalisation.

And eGo partners are keen to maintain momentum. Based on project results, they submitted two proposals. The first, to extend the project (under the code name H20) to largely deal with online automated application certification and identity management, was accepted and H20 is expected to start in 2015. The second, code named MUSE, addresses the H2020 call to help disabled people interact with the digital environment.

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9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
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CA402 | Innovative power technology gives industry and the environment a huge boost [THOR]

The THOR project has developed highly efficient, integrated and reliable power electronics technologies, offering major European industries new opportunities, steep growth in silicon carbide devices and increased competitiveness. Crucially, this project exploits new technologies for discrete power components and power cores, and systems – currently one of the most promising areas of electronics – while reducing CO_2 emission.

Innovative technology developed by the co-labelled CATRENE-EURIPIDES THOR project has produced a steep increase in silicon carbide (SiC) devices in the market and delivered solutions for packaging, cooling and electromagnetic compatibility. More compact power conversion solutions are expected in the key automotive, aeronautics and healthcare application areas. Importantly, all of this helps industry transform the SiC market from a device to a power modules business.

In modern power converters, most of the volume is taken up by cooling components and electrical filters. Now, SiC-based power devices take up less space, something THOR exploits in its development of high-temperature packaging, compact cooling systems and smaller filters. In addition, compact power-conversion systems with very high power density have been demonstrated in all three application areas.

THOR's main deliverables were:

- Highly reliable, design-oriented prototypes of miniaturised high-voltage, high-frequency and high-temperature power modules based on new wide bandgap semiconductors, like SiC;
- High-temperature SOI or SiC drivers and DC/DC converters using improved silicon-based power devices.

Market, environmental and societal spin-offs

In its goals to develop highly efficient, integrated and reliable power electronics technologies for automotive, aeronautics and healthcare applications, THOR worked widely with end-users from these three industries, together with European semiconductor, packaging and cooling manufacturers associated with technology developers, as well as European academic partners. Such broad collaboration was made possible by the unique assistance provided by two large European support-programmes: CATRENE and EURIPIDES.

THOR is expected to make all these technologies – ranging from power electronics components to complete systems – available in Europe, thus improving the robustness and reliability of high power electronics in the process, and facilitating their miniaturisation. This will also create new applications in the automotive, transport and healthcare sector. Critically, it will also increase the competitiveness of the major European industries in these fields, together with the European industry of power electronics, currently one of the most promising areas. In particular, THOR will contribute in sustaining a competitive environment for the European automotive industry by speeding up the

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Partners:

Airbus Group Innovations
Ampère Insa Lyon
Bruco Integrated Circuits
Cirtem
Epsilon Ingénierie
Labinal Power Systems (Safran)
NXP
Philips
Prodrive
Soitec
ST Microelectronics
Thales Microelectronics
Université de Versaille Saint-Quentin en Yvelines
TU/e
Valeo

Project leader:

Mark van Helvoort
Philips

Key project dates:

Start: October 2010
End: March 2014

Countries involved:

France
The Netherlands

Project website:

http://www.thor-project.eu/

PROJECT CONTRIBUTES TO

Communication	
Automotive and transport	✔
Health and aging society	✔
Safety and security	✔
Energy efficiency	✔
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	
More than Moore	
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Technology node	

time-to-market and reducing costs for end-users. In general, the transformation of the SiC market from a device to a power modules business will lead to a jump in growth of SiC devices: from 26% to 39% by 2015.

Away from the technology and economic spotlight, there are important societal issues which THOR addresses. For instance, these compact and highly efficient converters can be effectively deployed in meeting such environmental challenges as dealing with CO_2 emission and over-reliance on fossil fuels. Power converters will also reduce significantly the weight of cabling in an aircraft, thus reducing fuel consumption. And an additional 30% fuel is saved by storing transient energy during braking. In the medical area, more compact systems at a lower cost help to deal with health challenges in the ageing society.

Scoring commercially

Key to THOR's success is the way it leverages economy of scale by addressing its full supply-chain – from semiconductor-device producer to power system-integrator – in all three application areas. The commercial advantage is a stronger competitive environment for the various industrial partners, because recent advancements in power electronics technology provided by its academic partners have been integrated into advanced applications. This ranges from SiC and silicon-on-insulator (SOI) technology to full compact power converters integrated in large systems.

Encouragingly, THOR's industrial partners have already started reaping the fruits of their labour:

- The first products based on THOR technology are already available on the market. In September 2012, SiC diodes for photovoltaic converters were released. In 2014 this range will be extended to additional applications, and SiC Mosfets will follow soon;
- A new SOI process is in place, facilitating the design of high temperature drivers, and the integration of low-voltage and high-voltage integration at a lower cost;
- In the area of electric vehicles, a compact air-cooled high-voltage DC/DC-converter with an efficiency of 93% and 95% over a very broad output power range was demonstrated. The vapour chamber and heat sink have been designed such that the cooling capabilities of the converter are independent of the mounting orientation, thus offering wide flexibility to car designers;
- Four partners were able to offer a compact power converter which covers a very large temperature range, thus ensuring it can be suitably located on aeronautic engines and airplane brakes (which generate very high temperatures);
- Two other partners demonstrated the capabilities of full digital control for power electronic: among others, a compact high-voltage power supply with an ideal topology for introducing SiC components. Pilot tests in hospitals are already ongoing. In addition, a feedback system was developed which can correct up to 10 dB variations in amplifier gain.

Broad collaboration

Information sharing and cross-fertilisation – crucial to the success of the wider effort and future of a project such as THOR – was excellent and worked well within the project consortium: more than 70 reports (including results), have been internally exchanged; and new, long-lasting, collaborations have been established. Furthermore, the key project players in THOR have guaranteed their efficient and effective cooperation with other related European projects.

THOR also shared its newly acquired knowledge externally with those in industry and academia: more than 30 papers have been written; some 25 presentations were given; and 12 patent applications have been submitted. In addition, a book on the electromagnetic compatibility (EMC) of large systems and installations has also been published in Dutch and is currently being translated.

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9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

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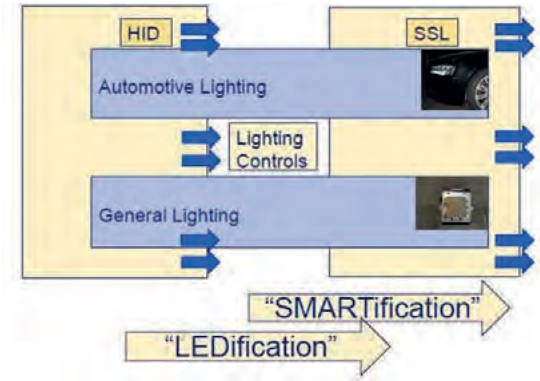
Cluster for Application and Technology Research in Europe on NanoElectronics

CA502 | Key lighting technologies drive energy efficiency and dynamic lighting [SEEL]

seel Solutions for Energy Efficient Lighting

Pressure by the European Union to phase out traditional incandescent technology and less efficient types of halogen lamps, together with a keen desire by lighting companies to improve energy-efficiency in lighting, were the driving force behind the SEEL (Solutions for Energy Efficient Lighting) project. They played a crucial role in the development of energy-efficient and dynamic-lighting systems, based on the high-intensity discharge lamp and solid state lighting, for general and automotive lighting for the professional market.



Prior to the SEEL project, incandescent lamps were receiving a bad press for their inefficiency and very short lifetimes. On the other hand, halogen lamps (a variant of the incandescent lamp) offered enhanced light output and double the lifetime, with efficacies of 10-25 lumen per watt (lm/W). And tubular fluorescent and high intensity discharge (HID) lamps had demonstrated efficacies of up to 100 lm/W, and emerging solid-state lighting (SSL) sources' were in the range of 30-60 lm/W. Importantly, these technologies, also capable of energy-consumption reductions and lower CO_2 emissions, could potentially boost the efficacy of the lighting system by a factor of five.

At the time, however, these HID- and SSL-based lighting systems still could not match the capabilities and characteristics of the halogen systems used in general lighting and automotive applications. Halogen lamps were well-known and accepted for such benefits as light quality, easy and deep dimming, instant-on light, small system size and their low initial cost.

Against this backdrop, the European Union issued its Energy-Using Products (EuP) directive (which took effect in 2009) to phase out all incandescent light bulbs and low-efficiency halogen lamps from the market by 2012 at the latest. This led lighting companies to search for ways of improving energy efficiency in lamps and find viable alternative light sources in order to meet legislation supporting the EuP directive.

Smart and green

SEEL's objective was to develop energy-efficient, dynamic lighting systems based on HID and SSL technologies for general lighting (initially for retail and hospitality) and automotive lighting, particularly for the professional market. Smart and energy-efficient electronics, also capable of reducing pollution and costs, were the key enablers in delivering desired performance improvements (and other objectives), as were standardisation, intelligent driving schemes and component integration.

Key to the project were four demonstrators that provided the required technology and applications to demonstrate and validate project results and deliverables. Lighting systems, for example, were developed to demonstrate the improved performance and successful integration (in a luminaire or system) of breakthroughs in lamps, drivers, controls, and optical and mechanical aspects. Some prime examples of these innovations are found in the use of spotlights in

ENERGY-EFFICIENT DEVICES AND ENERGY CONTROL SYSTEMS

Partners:

Audi
B+W
BAG
BESI
BIC
(LEFT THE CONSORTIUM)
Bochum Uni, CEA-LETI, DCD, Elmos, Infineon, IZM, Modular, NXP (DE), NXP (NL), Osram, Philips Automotive Lighting (DE), Philips Lighting (NL), Philips PL (FR), Philips Research labs Eindhoven, Philips Turnhout, TU Delft, TU/e, ULIS, Valeo.

Project leader:

René de Zwart
Philips Lighting

Key project dates:

Start: November 2010
End: October 2013

Countries involved:

Belgium
France
Germany
The Netherlands

Project website:

http://www.seel-project.eu/

PROJECT CONTRIBUTES TO

Communication	
Automotive and transport	✔
Health and aging society	
Safety and security	✔
Energy efficiency	✔
Digital lifestyle	✔
Design technology	✔
Sensors and actuators	✔
Process development	✔
Manufacturing science	✔
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the retail and hospitality segments, and front-end automotive lighting. A fifth demonstrator catered to the future use of controls to further reduce energy consumption through the advanced features of presence and activity detection.

Shining examples of collaboration

SEEL's project partners from four European countries contributed to strengthening the position of Europe as a global knowledge-centre, as well as its competitive position, particularly in the field of lighting.

There are also good examples of synergy and increased effectiveness. One is SEEL's collaboration with the SCHELP project (dealing with mercury-free lamps), where both projects required an accurate description of the properties of (near-) equilibrium plasma in complex mixtures. Another example is the deployment of SSL driver technology to control SEEL-designed lamps, as well as the small form-factor LED ones used in the ENIAC CSSL project.

Benefits of collaboration are notably apparent with SEEL's academic partners. The large store of experimental data and theoretical knowledge this project generated on ignition processes, plasma-cathode interaction and discharge physics can, in fact, form the basis for further developments. Furthermore, work emanating from SEEL is well documented and is expected to find its way into PhD and master theses, as well as, scientific articles. Apart from the direct benefit, methods devised to obtain the results will also be accessible and available for further work beyond this project.

The future looks bright

Both of SEEL's lighting markets look promising. In general lighting, replacement of incandescent and halogen lamps by energy-efficient light sources has resulted in large energy savings. Affordable HID light sources and drivers with a luminous flux above 4000 lm (with dimming and hot re-strike options) will continue to be prominent players in the lighting market for the foreseeable future, securing the manufacture of HID lamps and control gear in Europe and related jobs.

In automotive, the adoption of highly efficient lighting in cars is directly driven by the reduction of pollution, where governments have defined legal requirements to cut CO_2 emission of cars. Halogen, HID and LED technologies are predicted to share the lighting market as we move towards 2018-2020, after which HID will continue to play a significant role. And automotive lighting will not experience an abrupt global change of technology, rather a shift in segmentation: while LED starts to replace HID for the top segment, HID lighting applications will shift towards mid-segment cars.

Furthermore, there will be a mass replacement of automotive halogen lamps with xenon HID ones, leading to lower fuel consumption and safer driving. This move will also create a new business with considerably increased volume, thus securing the future production of xenon HID lamps and control gear in Europe, as well as development and manufacturing jobs.

SEEL project partners are also starting to benefit directly. The flat spot developed in the SSL General Lighting work package has generated momentum as a potential successor to a lighting product from a French SEEL project partner. New-generation lighting systems with intelligent lighting control developed in SEEL are also expected to contribute to global energy savings and lower CO_2 emissions, but without sacrificing well-accepted properties of existing lighting solutions.

And standardisation in both light source and intelligent control – something to which SEEL assigned a high priority – is expected to create high-volume applications as existing lighting sources are replaced. By increasing volume demand, standardisation will reduce costs, as well as ensure a leading position for the European lighting industry, now and in the future.

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CT205 |

Key embedded NVM products give European suppliers a competitive and technological advantage [REFINED]

Despite the complexity in developing embedded non-volatile memory (NVM) products, and the dire economic situation, increasingly more competitors are trying to enter this arena. To counter this threat and maintain its competitiveness and technological superiority, Europe has not only been developing solutions based on Moore's law's technology-shrink path, but also studying low-cost approaches and innovative cell concepts. Now, thanks to European leadership in this field and the REFINED project (and previous related projects), the first embedded non-volatile flash memory products deploying 65/55 nm, as well as the introduction of the 45 nm technology nodes and some low-cost options have been released.

Non-volatile memory (NVM) technologies play a crucial role in developing reliable, high-performance microcontrollers used in various applications, including smart cards, and in the automotive and consumer electronics sectors. There is now a notable effort in Europe to integrate NVM into baseline CMOS technologies, creating programmable product platforms for a more generic system-on-chip (SoC), and thereby increasing European chipmakers' competitiveness in derivative technologies. Embedding flash memory in SoC devices facilitates the use of application-specific software in more generic SoCs, thereby combining volume production with product differentiation.

The main goals of REFINED were to:

- Integrate NVM options in deep sub-90 nm standard CMOS baseline technologies, without performance degradation of the baseline CMOS;
- Integrate flash with 55 nm CMOS logic on 300mm wafers;
- Bring innovative cell options, such as nanocrystals, or process options, like high-K dielectric, closer to industrialisation through close cooperation between research and industry partners;
- Develop new low-cost cell solutions aimed at overcoming current limitations, such as endurance, without increasing the overall process cost;
- And develop test structures and methodologies to characterise and verify analogue performance of embedded NVM technology platforms.

Meeting milestones

Work in REFINED was divided into three main areas:

- Technology development of 65/55 nm and 45 nm eNVM processes, and low-cost eNVM processes for existing technology nodes;
- Developing new modules and cell concepts: focusing on the introduction of innovative elements in the process, namely high-k dielectrics, silicon nano-crystals and disruptive technologies; and conducting a benchmark and state of the art investigation into the various options;
- IP development, testing and characterisation: dealing with the design and layout of the various test structures, macro-cells and demonstrators; and tackling the issue of reliability and testing at intrinsic cell level.

And REFINED met all its milestones:

- Preliminary work for the development of the 45 nm new floating gate memory is complete and 55 nm eFlash technology has passed the qualifications steps successfully and is ready for production;
- Three eFlash technologies (from 90 nm to 150 nm) are in the production phase and a roadmap has been defined for the 65 nm embedded memories;
- Development of the LF110 CMOS core process with two embedded memory options (SST and single poly NVM) is proceeding according to plan.

CT205 | Key embedded NVM products give European suppliers a competitive and technological advantage [REFINED]

Partners:

ATMEL
CEA-LETI
Infineon Technologies
LFoundry Rousset
STMicroelectronics

Project leader:

Dominique Goubier
STMicroelectronics

Key project dates:

Start: January 2010
End: December 2012

Countries involved:

France
Germany
Italy

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	✓
Health and aging society	
Safety and security	✓
Energy efficiency	
Digital lifestyle	
Design technology	
Sensors and actuators	
Process development	✓
Manufacturing science	✓
More than Moore	✓
More Moore	
Technology node	

European co-operation and leadership

REFINED brought together major R&D actors – chipmakers and research organisations – to develop the 65/55 nm generation, as well as improve the current 90 nm generation through technology shrink. In addition, this project supported the broad IP portfolio of project partners by reducing the time required to validate and industrialise new NVM cell concepts and process options. For this, REFINED relied on close co-operation between its industrial partners and research centres, in which reuse of existing technology platforms for industrial validation of the new concepts and process options was central. The variety of solutions studied will enrich the European offering and capability to fulfil any possible market requirement. The final goal is to maintain and consolidate the leadership of European companies in offering the most advanced embedded NVM SoC solutions worldwide.

Cross-European co-operation was a prerequisite for a successful completion of this challenging project, especially since the knowledge and competences of the different partners are complementary and cannot be found within a single European country. Usefully, the partners had already worked together in MEDEA, MEDEA+ and EU Framework Programme projects, which focused on embedded NVM and analogue process options, from 180 nm down to 90 nm baseline CMOS, with preliminary research into 65 nm and 45 nm cell concepts and process options. This project was in fact built on this long European co-operation and the good results achieved notably in the MEDEA+ MaxCaps project and, in the more design-oriented ENIAC JU SMART project essentially based on phase-change memory.

European leadership in embedded NVM is well recognised. In recent years, consortium partners have released the very first embedded NVM products for 180 nm, 130 nm and 90 nm technology nodes. These were based on work done in previous international co-operative projects. The target and present forecast is that one of the partners, a key semiconductor supplier, should be able to be the first to announce the availability of a 55 nm embedded flash technology working with 300 mm wafers.

For products with a large memory-to-logic area ratio – such as subscriber identity module smartcard products for mobile phones – it is expected that 90 nm shrink technologies using 200 mm wafers will be very cost-competitive with respect to 65 nm technology. A REFINED partner is working on such an intermediate technology node, and expects to be the first in the industry able to offer such products.

And shrinking embedded, single, poly-electrical erasable programmable read-only memory (EEPROM) at 150/130 nm using 200 mm wafers is a very cost-competitive way forward for devices requiring a moderate NVM size, and which need optimally stored information granularity demanded for applications targeting code access (such as nomadic applications, smart cards and industrial control).

Now, despite the increasing shift of manufacturing operations towards low-cost areas, the increase of added-value in SoC products (made possible as a result of REFINED) will allow European companies to lower manufacturing costs. In addition, they will be able to be more focused on other innovative products, which represent reliable, high-margin opportunities.

And the collaboration seen in REFINED is set to flourish beyond this project. Consortium partners in Grenoble and Dresden continue to participate actively in the two nanoelectronics clusters established at these locations in March 2010, further strengthening their co-operation in advanced technologies and industrial processes.

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CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

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CT206 | All-in platforms for cost-effective design and production of CMOS 32/28nm technology [UTTERMOST]

The UTTERMOST project brought together an alliance of European industrial businesses to offer total design, development and production platforms for CMOS 32nm and 28nm technologies. In doing so, UTTERMOST is providing ample opportunities for European companies to respond to an explosion in new portable devices with amazing technological capabilities and bandwidth-intensive multimedia applications. Crucially, this project will strengthen the competitiveness of European industry by providing complete solutions for low-power communications-centred, multi-core architectures.

UTTERMOST was built on earlier research done at the International Semiconductor Development Alliance (ISDA) and in the FP7 project PULLNANO. The latter demonstrated the feasibility of an SRAM 6T cell deploying 32nm design rules and e-beam lithography, and using FinFet transistor architecture (FinFet is a non-planar, multi-gate transistor built ether on bulk or on SOI substrate) and extreme ultraviolet at the IMEC research centre. In fact, all this prior research can be seen as the preparation phase in creating a new European CMOS technology node. The second phase – the UTTERMOST project – is largely the development phase leading to production and industrialisation.

All-inclusive approach

UTTERMOST represented a joint effort by major players in the European semiconductor ecosystem (operating around three leading semiconductor companies), working at the leading edge of technology. They collectively generated advanced-process modules and validated – at two European manufacturing facilities, deploying four product demonstrators designed by three application providers – a design platform for reliable CMOS 32/28 nm digital memory technologies based on 300 mm wafers.

In short, technology enablement was achieved through:

- Test-mask development for process validation;
- Extended library design and modelling;
- Design methodology enhancement and portability/scaling of libraries;
- Assessment of the integration choices in four major demonstrators.

UTTERMOST's key achievements and deliverables were:

- A technology node with two low-power (LP) design platforms and design enablement for 32nm and 28nm;
- Four complex demonstrators which validated the LP design platforms;
- A site for prototyping and industrialising a 28nm bulk LP CMOS using HK/MG gate (high permittivity gate dielectric with metallic gate electrodes) first, followed by innovative back-end-of-line (BEOL) – the second part of IC fabrication – for up to 10 metal levels. A second source-plant was also qualified.

Experience and expertise gained from the 28nm LP technology was crucial in the subsequent development of 28nm FDSOI technology and conversion methodology (from 28nm LP to 28nm FDSOI including the porting of the 28 LP libraries). In addition, the yield ramp of 28nm LP resulted in a much faster time-to-manufacture for 28nm FDSOI technology.

Qualification (industrial maturity) of the 28nm LP technology was achieved and the 32nm and 28nm technologies reached all their targets in terms of device performance and integration density, as well as, reliability. And design platforms met their dynamic and static power and speed targets.

Notably, complete design enablement of the 32/28nm technology node required individual validations for the 32nm version, and subsequently for the 28nm one. And the development effort did not stop at platform level. In fact, the work required to develop marketable products was significantly

Partners:

Cameca
CEA-INAC
CEA-LETI
CNRS-LTM
CNRS/CEMES
Dolphin Integration
Fraunhofer Institutes
GLOBALFOUNDRIES
IBS
INPG/IMEP
Intel Mobile Communications (formerly a division of Infineon Technologies)
SERMA Technologies
ST-Ericsson
STMicroelectronics
Thales Communications
University of Stuttgart

Project leader:

Gilles Thomas
STMicroelectronics

Key project dates:

Start: January 2010
End: May 2013

Countries involved:

France
Germany

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✓
Digital lifestyle	✓
Design technology	✓
Sensors and actuators	
Process development	✓
Manufacturing science	✓
More than Moore	
More Moore	✓
Technology node	✓

higher than to develop the technology platform. That is why it was imperative to deploy product demonstrators.

Impressive European industrial and institutional support

Worldwide, the digital CMOS manufacturing industry is being streamlined, with increasingly fewer actors involved in digital CMOS. Crucially, UTTERMOST offered Europe a rare opportunity to put together such a large consortium for the purpose of industrialising a mainstream, leading-edge 'More Moore' technology.

The project consortium comprised 19 French and German partners which included major chipmakers, equipment manufacturers and research institutes. Project goals could only be met because of Europe's strong industrial and institutional bed of knowledge, experience and expertise in modelling, simulation and powerful physical and electrical characterisation tools to fully understand such sophisticated, state-of-the art technologies.

A position of strength

UTTERMOST is expected to strengthen the competitiveness of European industry by providing complete solutions for low-power communications-centred multi-core architectures. It will also contribute to new business development and boost Europe's position for innovative applications, particularly in communications components and chipsets using 32nm CMOS computing and storage power.

With project details widely available through some 168 publications, conference papers and one doctoral thesis, research organisations and academic teams will gain intellectual property and process module knowledge on industrial lines, enabling them to extend their influence and draw interest from industrial partners.

UTTERMOST's success also strengthens the position of equipment suppliers and enable them to innovate (eleven patents were filed) and expand further their product portfolio for silicon industry applications. This project will also provide ample opportunities for European companies to continue participating in the most advanced high-speed interfaces for new product creation. Such products will power portable devices that will define a wireless century characterised by pervasive broadband wireless communications and networking. This transformation is being driven by an explosion in bandwidth-intensive multimedia applications, as well as by the expanded technological capabilities of personal communications systems, air interface technology, IP networking and new architectures, such as mesh networking.

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CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

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CT207 | D/TSV integration platform goes a long way in successfully meeting IC manufacturing challenges [COCOA]

As the semiconductor manufacturing world faces significant challenges integrating heterogeneous technologies, there is a call for the industry and R&D institutions to collaborate to ensure the industry meets its goals in a timely manner. That is why the COCOA project was keen to develop a complete and mature 3D integration technology platform covering the entire range of processes required – from vertical interconnects and robust bonding to innovative packaging approaches – to address a wide range of products.

For decades, Moore's law has predictably driven silicon scaling, and semiconductor manufacturing has been based largely on planar (2D) technology. However, increasing need for less power, smaller form-factor and higher performance continues to drive ICs towards 2.5D and 3D.

The main objective of this project was to achieve chip-level three-dimensional, through silicon via (TSV) integration, wafer-to-wafer and die-to-wafer bonding, and packaging of stacked circuits, in order to create a complete technological platform for high performance and cost-effective 3D system manufacturing. The stacking, interconnecting and packaging technologies of 'multiple chip-on-chip' will open new opportunities in Europe in terms of applications and performance.

An impressive first

COCOA specifically addresses:

- 3D interconnects shrink and related specific development-process steps to increase density and cover the existing gap between medium (104 cm^2) and high-density (106 cm^2) technologies;
- 3D performance (thermal, mechanical, electrical and the like) improvement;
- Creating product demonstrators: specific prototypes developed for multimedia and wireless applications as well as sensor-integration applications which open new manufacturing opportunity to European partners.

And COCOA's technical results are impressive:

- The first real 3D integration of a processor with a wide I/O memory interface (WIOMING) was realised in 2012, with excellent results;
- Some of the most challenging steps for sensor integration with a μhot plate were achieved;
- Bonding and debonding steps for thin wafers.

Achievement through collaboration

An excellent collaborative spirit was present right from the start (and some partners continue to work together even though the project has ended). Communications were efficient and effective. Well-attended face-to-face meetings and monthly conference calls facilitated informal discussions between partners, and proved to be excellent tools to exchange ideas and propose new experiments, driving innovation and creativity (COCOA generated 12 patent applications). In addition, 70-odd publications and (conference) presentations also helped with information dissemination and exchange.

There are several achievements worth mentioning. The WIOMING demonstrator was the first 3D integration of its kind. Furthermore, some milestones were reached ahead of schedule. CMOS-compatible integration of the gas-sensitive SnO_2 layer and the sensitive measurement of CO (10 - 90ppm) with a DC power consumption of only 23 mWatt is an impressive result: the state-of-the-art reports much higher power consumptions in the 100 mW to 1 W range.

Finally, despite the challenge of 3D integration bonding/debonding (especially for thin wafers),

CT207 | D/TSV integration platform goes a long way in successfully meeting IC manufacturing challenges [COCOA]

Partners:

ASM-B
Austrian Institute of Technology
Austriamicrosystems
CEA-LETI
Datacon
EVGroup
HFWN
IM2NP
Semitool
SPTS
ST-Ericsson
ST Tours
STMicroelectronics
TUW

Project leader:

Brigitte Descouts
STMicroelectronics

Key project dates:

Start: March 2010
End: June 2013

Countries involved:

Austria
Belgium
France
UK

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	
Health and aging society	
Safety and security	✓
Energy efficiency	✓
Digital lifestyle	
Design technology	
Sensors and actuators	✓
Process development	✓
Manufacturing science	✓
More than Moore	✓
More Moore	
Technology node	

COCOA was able to successfully demonstrate the direct bonding of thin wafer, using standard alignment equipment.

Reaping the benefits

COCOA delivered direct gains for project partners:

- Concepts successfully developed in COCOA for temporary and chip-to-wafer (C2W) bonding can also be used for future customer demonstration;
- A partner, who has become one of three main suppliers in the field of TCB equipment, expects a yearly revenue in TCB equipment of more than €10m following the launch of a new TCB bonder; another partner is expecting sales of its silicon photonic systems to reach $215m by 2017;
- COCOA provided a semiconductor supplier with a good opportunity to develop its very first 3D pilot line and demonstrate the benefits of moving to 3D. This means offering complete solutions for new applications requiring high performances, high density and/or highly heterogeneous systems;
- Thanks to the excellent reliability results that were demonstrated for TSV-Middle, this solution is being transferred to CMOS sensor pilot lines to address automotive applications with stringent reliability specifications and requirements;
- 3D/TSV applications are expected to show significant CAGR over the next years for specialised process equipment for which one partner has a suite of dedicated tools that will speed up the industrialisation of the 3D/TSV processes;
- COCOA development work and deliverables will help commercialise equipment at industrial sites once volume-production starts, though integration with upstream/downstream process steps, and mandatory cost-reduction needed to meet industrial requirements;
- And two partners' collaboration in temporary bonding resulted in the creation of a joint lab.

COCOA also delivered other market and industry gains. As a key enabling technology, three-dimensional chip systems integration has gained significant momentum. Over 50 companies have been involved in developing 3D interconnects, and surveys forecast that the market for 3D integration will increase at a compounded annual growth rate of 52%. Furthermore, the development of a 3D integration technology platform capable of sustaining product prototyping and industrialising multiple chip-stacking will contribute significantly to the preservation of European semiconductor industry activities and could even contribute to the re-localisation of employment from Asia to Europe. In addition, this innovative technology will create new opportunities by using the expertise of European companies in the fields of high added-value product design and manufacture.

Finally, the flexibility characterised by this approach will ultimately combine different technologies dedicated to highly-specialised, high-performance functions per layer by using front-end technologies available in Europe. This will make it possible to replace conventional system-in-package (SiP) solutions, usually integrated by Asian companies. The co-integration of multiple CMOS technologies will greatly extend production among 300 mm, 200 mm and even older European fabrication facilities as innovative 3D products will use dedicated technologies to achieve complex system integration.

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

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CALL 3

Cluster for Application and Technology Research in Europe on NanoElectronics

CA308 | Project delivers crucial imaging technologies [ICAF]

image capture of the future

Addressing future imaging requirements, the project ICAF researched, developed and demonstrated some key image capture, processing and transmission technologies. Launched in 2011, the project ICAF achieved major advancements in image capture technology and systems to further increase automation in high added-value production processes, state-of-the-art security systems, as well as, in the traffic and automotive areas. Of course, remaining at the forefront of image capture, transmission and processing is crucial for European businesses – especially ICAF's industry project partners – considering the range of applications that support important industries in Europe, which in turn have export markets beyond Europe.

Delivering state-of-the-art imaging elements and applications

ICAF researched, developed and demonstrated advanced image capture, processing and transmission technologies. The first set of deliverables in silicon development produced five chips:

- Image sensor test vehicle to test out the architecture and new intellectual property (IP) blocks (reusable, tested product-design outcomes which can increase design efficiency and quality);
- Three pixel-test chips used to evaluate over 1,500 different pixel variants to significantly improve noise and dark current;
- CoaXPress (an asymmetric, high-speed and coaxial serial communication standard) transceiver chip, which enables communication of up to 12.5Gbps per link (further improvements to increase the cable length are ongoing).

The next set of deliverables included algorithms and processing IP blocks needed for single lens 3D, increased pixel-rate image capture and a video over internet protocol for professional broadcast purposes. These comprise:

- Algorithms for improving the quality of video streams captured by professional 2D/3D cameras as in HDTV broadcasting and surveillance applications;
- Methods for depth-map generation;
- Single lens 3D micro-stereopsis algorithms;
- Improvements in JPEG 2000 compression for the Broadcast Profile standard that increases the efficiency of the code-stream;
- Video over internet protocol IP blocks to be reused in video over internet protocol applications.

ICAF also delivered four key applications that demonstrate and validate:

- Real-time single lens 3D image capture for professional broadcast: depth image-based rendering (DIBR) is added to the single lens 3D camera system, based on the newly developed stereo algorithms. This will allow the dual HD stream generated by the camera system to be absorbed in real-time through a frame grabber in the PC platform;
- Video over internet protocol transmission: which allows an uncompressed stream between a video camera to a base station on a 10G Ethernet fibre link;
- Machine vision (MV) camera platform for 3D

Partners:

Adimec Advanced Image Systems
Axon Digital Design
Delft University of Technology
EqcoLogic
intoPIX
Ghent University
Grass Valley Cameras
Hasselt University
ON Semiconductor Image Sensor

Project leader:

Jochem Herrmann
Adimec

Key project dates:

Start: October 2011
End: September 2014

Countries involved:

Belgium
The Netherlands

Project website:

http://www.icaf.tv/

PROJECT CONTRIBUTES TO

Communication	✓
Automotive and transport	✓
Health and aging society	✓
Safety and security	✓
Energy efficiency	
Digital lifestyle	✓
Design technology	✓
Sensors and actuators	✓
Process development	
Manufacturing science	✓
More than Moore	
More Moore	
Technology node	90nm; 180nm

metrology: used to test and evaluate the silicon developed in the project; together with camera hardware, high-speed processing and interfaces, as well as, frame grabbers to grab images for processing in MV applications;

- Security/surveillance camera platform and three multi-head camera systems: to test and evaluate the silicon developed in the project.

Commercially successful

Project deliverables will not only lead to the manufacturing partners producing new revenue-generating products, but they will also create intellectual property in the form of patents and innovative techniques and technologies. In concrete commercial terms, ICAF's R&D work (which won three awards) resulted in the first 3D single lens stereopsis camera and the first HDTV slow-motion, triple-speed camera that can continuously output a slow motion stream, together with a normal HDTV stream.

The project also introduced the next-generation CoaXPress transceiver solutions, and produced the first rugged surveillance camera using this standard. New methods, techniques and standards (for example, in video compression and automatic transformation of 2D images into 3D) will go a long way in strengthening Europe's position in state-of-the-art, high-speed and industrial imaging.

Important spin-offs as well

ICAF also has some less obvious, yet notable, benefits. Machine vision cameras in 3D media production and immersive internet interaction, for example, could enhance quality of life. Increasing use of 3D in machine vision applications could lead to research in image sensor and processing architectures for applications, such as automated optical inspection in electronics manufacturing. This will result in the next generation of technologies for cost-effective 3D metrology and inspection systems.

Furthermore, some of the technology demands in areas ICAF focused on could equally apply to other fields, such as automotive, which also need cameras for improved safety (distance monitoring, pedestrian detection, sleep detection and airbag control are just some examples). There is also a rapidly developing market for automated surveillance for use in the care of the elderly, an area of concern that address demographic trends.

Effective European collaboration and resources well spent

Importantly, ICAF was a European effort. Its nine-partner consortium comprised six European advanced-manufacturers and three European universities, all with specialist knowledge and experience in the new technologies and efficient use of synergies between these technologies. This consortium researched and developed key methods, intellectual properties, applications and products, while contributing to important standards, generating two patent applications and earning some five awards. The project has also been showcased at all relevant trade shows, and in papers presented at several conferences.

All this will not only benefit the project partners, but also business, consumers and research in Europe and beyond. After all, the industry project partners are important players in their respective European (and worldwide) markets. Products that incorporate results of the ICAF project are manufactured within Europe and shipped worldwide. Moreover, researchers and scientists at the three participating universities will ensure the knowledge and experience gained will be widely shared and productively used.

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CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
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PROJECT RESULTS

CA403 | Combining design solutions ensures future systems-on-chip reliability [RELY]

Systems-on-chip (SoCs) become more complex and prone to failure as the integration of new functions and devices increases, dimensions decrease, and operating conditions get more extensive. In addressing these issues, the RELY project found ways and means to maintain reliability and risk at acceptable levels.

One of the main problems with integrated circuits (ICs) approaching atomic dimensions is the high susceptibility to miniscule interferences and deviations. Each new generation leads to larger production fluctuations and ageing, which deteriorate properties and therefore the functionality of new systems-on chip (SoCs). Their complexity is rapidly increasing as more functions, devices and sensors/actuators get integrated, and operating conditions become more extensive. However, safety-critical components still have to remain reliable, despite increasing ageing and failure sensitivity.

Managing reliability while reducing dimensions and costs

Mainly focusing on the avionics, automotive and medical fields, RELY's two main objectives were to ensure future SoCs reliability by combining different solutions along the entire value chain; and to make SoCs that have a new level of functionality and complexity through increased reliability possible for a reasonable price. In addressing these issues, the RELY project has also made risk less of an academic issue, and more predictable and manageable.

These application-based goals can be translated into the following product development areas of focus:

1. Prediction of reliability at all phases of system design;
2. Design and architectural solutions that increase system reliability;
3. Reducing chip dimensions and cost-overheads.

In early and fast reliability-prediction, RELY's research led to a combined model for two of the most relevant effects: Negative Bias Temperature Instability (NBTI); and Hot Carrier Degradation (HCD). For three further relevant effects – Time Dependent Dielectric Breakdown (TDDB), Soft Breakdown (SDB), and Electro-migration – the models have been characterised by, and evaluated against, silicon measurement-data, thus increasing the model's accuracy significantly.

In addition, RELY delivered two new methodologies: to select optimal design parameters (in terms of functionality as well as reliability) for analogue circuits; and to generate degradation models for all available tool interfaces directly from the characterisation data (thus simplifying drastically the effort to establish a degradation model out of the measurement data, and allowing commercially available tools to be used).

Increased system reliability

RELY also developed several run-time reliability-management strategies (using these prediction methodologies), such as sensor redundancy schemes; run-time degradation sensing; sensor output data aggregation; and reliability management using a dedicated reliability layer, or selective hardening techniques.

The project also presented a highly reliable high-temperature technology which increases electro-migration susceptibility. In addition, it developed techniques to prevent fatal field returns due to early detection in the design process far before tape-out; and a new methodology and circuitries which can detect quality problems in the fab hundred times faster.

Reduction in size and cost issues

Thanks to the overdesign of its reference circuit, RELY was able to demonstrate a reduction of 20% in power overhead in the analogue part of a test chip used in medical devices, and a 37% reduction in the digital part, when subject to the

PROJECT CONTRIBUTES TO

- Automotive and transport
- Health and aging society
- Design technology
- Sensors and actuators
- Manufacturing science
- More than Moore
- More Moore

Technology node / 350nm to 28nm

PARTNERS

Atmel
CEA LIST
EADS
Fraunhofer
Infineon
Intrinsic-ID
ITTP
MunEDA
STMicroelectronics
TUM
UHB ITEM
X-FAB

COUNTRIES INVOLVED

- France
- Germany
- Romania
- The Netherlands

PROJECT LEADER

Georg Georgakos
Infineon Technologies

KEY PROJECT DATES

May 2011 - April 2014

www.rely-project.eu

same reliability target. The project also developed a redundant (thus highly reliable) sensor array for avionic applications in extremely harsh environments, demonstrating how to build reliable systems from unreliable components, especially sensors. These techniques can also be used to maintain the required reliability at lower costs, rather than further increasing it. Under these constraints, it is possible to find solutions that ensure high reliability, while minimising the design overheads in terms of area, power or performance. All these will finally reduce the cost of a reliable system – making smaller, more powerful technologies more attractive for reliable systems, and thus ultimately leading to improved, and even completely new, reliable systems.

Finally, in addition to demonstrating actual cost-reduction, the project also improved the design methodology to generally reduce the cost of reliable system design. A better understanding of the correlation between NBTI and HCD led to an improved validation methodology. The 'pessimism' of long-term NBTI and HCD prediction can be reduced by a factor of two, generally leading to a huge cost-reduction by avoiding unnecessary overdesign. A methodology was also developed to optimise yield and reliability of analogue circuit blocks automatically and ultimately reduce costs.

Impacting key European industries

In providing a better understanding of ageing due to various reliability mechanisms, RELY addressed the special semiconductor requirements of the aeronautics, space and defence industries. In particular, applications in aeronautics need an extremely high level of robustness, reliability and quality. The impact will also be felt in other domains where high reliability is critical. For example, SoC applications in avionics, medical, industrial automation, and where automotive and telecom infrastructure requires uninterrupted operations. Another example is in the medical area, where new high-reliability implantable devices operate under difficult (low power) conditions – a new field of business opportunities.

RELY is considered a well-recognised European project, addressing the central issues of European integrated device manufacturers and application designers. Thanks to this and other European and national projects, Europe is clearly dominating worldwide research in terms of ageing effects, robustness, and reliability: The project is therefore of broad relevance to major European industries, and its results will strengthen the established position of the consortium partners in their specialist fields, while the dissemination of the results will ensure broad distribution of the new methodology.

RELY's strong position takes research to the next step

RELY's technical achievements have resulted in four patents, two books and articles in 14 trade journals. The project was represented at 114 trade fairs and numerous tutorials, and project participants were invited to talk at conferences and contribute to workshops.

Notably, RELY's position is further strengthened by a total of eight direct or indirect national and European follow-up projects, reinforcing and expanding RELY's research base in such fields as standardisation. Importantly, in taking into account such additional physical aspects as the coupling between variation and degradation, these new follow-up projects will firmly bind RELY's research to the needs of specific target applications, like automotive safety.

CATRENE Office
9 Avenue René Coty
F-75014 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

Cluster for Application and Technology Research in Europe on NanoElectronics

CT208 | FDSOI transistor architecture qualifies for 14nm node CMOS technology [REACHING22]

With the semiconductor industry leader announcing its choice of transistor architecture – 22nm based on a fully-depleted (FD) 3D FinFET architecture built on bulk silicon – European industry urgently needed to assess the optimal transistor architecture for the 22nm node. The REACHING22 project was therefore launched to investigate fully-depleted devices at 22nm versus conventional planar transistors on bulk silicon, and the benefits they offer in low-power applications. This project is now coming to an end, having made significant progress towards meeting all its objectives, and with encouraging results: the 'winning' technology – called FDSOI – uses a planar FD transistor architecture built on a silicon-on-insulator (SOI) engineered substrate.

Although bulk CMOS technologies are reaching some intrinsic limits with gate lengths drawn below 25nm, the major issue is the need to scale geometries further while keeping acceptable dynamic and static power, on one hand, and device variability at ever lower operating voltages, on the other. The REACHING22 project researched the optimal transistor architecture and its integration for 22/20nm node core CMOS technology, and provided an electrical proof of concept.

Meeting all objectives

The overall objective of REACHING22 was to create appropriate conditions for the deployment of CMOS 22/20nm technologies in Europe. More specifically, this project's technical goal was to research the optimal architecture and integration path for the 22/20nm node core CMOS technology, aiming at an electrical proof of concept based on an initial test mask set. Although REACHING22 covered the first phase of the 22/20nm technology deployment, the test mask set goes well beyond the simple proof of concept, traditionally based on an elementary SRAM cell.

Preliminary assessment work on the FDSOI technology performance was conducted using previous-generation design rules (28nm) and a test mask. At the same time, the necessary process modules for the 22/20nm technology and an appropriate silicon-on-insulator (SOI) substrate for the 20nm node were being developed. Subsequently, an electrical benchmark comparison was conducted between the 20nm bulk and the 20nm FDSOI CMOS technology architectures, based on transistor performances and an initial evaluation mask set.

REACHING22's key objectives (which were fully met) were:

- To demonstrate the 28nm FDSOI transistor architecture. Here a 40% performance boost (at Vdd of 1V) was attained, compared to equivalent lithography planar bulk transistors. Performance gain was even higher at low operating voltages (100mV reduced Vmin on SRAM), leading to the decision to industrialise the 28nm FDSOI technology and to develop a fully-fledge design platform. Variability of FD NMOS on SOI was reduced by 40% compared to bulk NMOS;
- To design and develop a complex SoC (application processor) demonstrator of 69mm^2 in 28FDSOI to serve as a qualification vehicle for the technology. This resulted in an outstanding dynamic performance over an extended supply voltage range;
- To achieve 100% toolset compatibility with 28nm bulk by extending the lifetime of the current toolset in the manufacturing fab.

Leadership through innovation

These encouraging results led the consortium to seriously consider FDSOI architecture as the major technology option for the 20nm node, displacing the 20nm bulk concurrently under development, and which could not show a comparable power-performance advantage. (Considering 20nm FDSOI is also capable of delivering next-node performance, it was decided to name it 14FDSOI.)

FDSOI technology offers several advantages. It has, for example, the potential to address the cost-per-formance squeeze facing the 22/20nm node as long as substrate materials are available in adequate volume, quality and price. FDSOI also provides a low-risk option for semiconductor companies seeking to take advantage of the benefits of

Partners:

CEA-LETI
INPG/IMEP
CNRS/LTM
SOITEC
ST-Ericsson
STMicroelectronics
Université Catholique de Louvain (UCL)

Project leader:

Gilles Thomas
STMicroelectronics

Key project dates:

Start: April 2011
End: March 2014

Countries involved:

Belgium
France

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	
More Moore	✔
Technology node	22/20nm

fully-depleted transistor architecture, while leveraging existing design and manufacturing capabilities. Although SOI substrates increase the overall technology cost, it can be compensated by devising an integration scheme less demanding in operational steps, while still maintaining a multi-Vt offer. FD transistors can also solve scaling, leakages and variability issues associated with shrinking. Globally, the resulting CMOS technology is less complex and therefore enjoys a good manufacturability and yield. And system-on-chip (SoC) devices, such as high-performance, low-power wireless multimedia processors, exhibit different requirements from mono-functional processors plugged into the mains.

REACHING22 has maintained a vibrant ecosystem in 'More Moore' technology, essential for developing strategic state-of-the-art digital electronics, especially low-power electronics needed to conserve energy and extend battery life in handheld devices. It will also provide accurate analytical and technology computer-aided design models to help with the development, assessment and optimisation of the different technology options. Several test structures will also be implemented on silicon to assess FDSOI technology for SoC and ultra-low-power applications.

Comprehensive and coherent strategy

Through this strategic project, 22nm node technologies, process modules and the screening of possible options were actively investigated with the ultimate goal of introducing them into industrial production in 2014 or 2015, at the latest. This means the various actors can deal with the challenges of worldwide business requirements and consolidating their leadership in a key enabling technology, instrumental to the communications sector.

Now, with 22/20nm core CMOS technology at a crossroads and with the need for innovation to keep this technology moving forward, a continuous and sustained effort is of paramount importance to the health of this sector in Europe. That is why REACHING22 is part of a series of More Moore projects, which constitute a comprehensive and coherent strategy in the development of successive digital CMOS technology nodes. With REACHING22 completing all its milestones, the initial research phase on the 20/14nm node technology is being concluded. However, the design enablement phase – in the form of the CATRENE DYNAMIC-ULP project – is already in progress, with the objective of deploying a low-power design platform. Furthermore, the ENIAC PLACES2BE project provides a pilot line for 'productisation' and a path to the industrialisation of '2X-1Xnm' FDSOI technologies in Europe.

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CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

PROJECT RESULTS

CT209 | Advanced silicon platforms for RF, MMW and THz applications a reality [RF2THZ SiSoC]

Having first investigated the potential and capabilities of three silicon system-on-chip advanced technology platforms – radio frequency (RF), millimetre-wave (MMW) and terahertz (THz) – RF2THz project then developed critical electronic components and application demonstrators required by the consumer industry and by such diverse disciplines as health science, telecommunication, genetic screening, security and industrial automation.

There is no area of modern life untouched by the progress of microelectronics. Thanks to its advances, new market opportunities are emerging in Europe, characterised by the need for products and services offering both mobility and connectivity. Europe has a solid industrial base, especially in telecommunications, home electronics and automotive, and is well profiled for this future growth. This is reflected in one of the aims of the RF2THz project – to establish a European approach for gigabit data communications and automotive radar developments, which improve European competitiveness against USA and Japan vendors.

Key technology platforms with demonstrators

Using results obtained from several previous MEDEA+ projects as its basis, RF2THz investigated the potential and capability of three advanced technology platforms: 55nm SiGeC BiCMOS from STMicroelectronics; the newest NXP BiCMOS which integrates Elite Passive devices; and the photonic devices based on the IHP SiGe BiCMOS.

It subsequently developed silicon technology platforms for emerging radio frequency, (RF), millimetre-wave (MMW) and terahertz (THz) consumer applications, such as:

- 77/120 GHz automotive radars;
- MMW imaging and sensing, fast-measurement equipment;
- 60 GHz wireless networking and fast-downloading systems;
- 400 Gbit/s fibre optics data communications systems;
- 4G photonic mobile communications and high performance RF wireless communication systems;
- Two-way satellite communications;
- Label-free biosensing.

In addition, findings were also deployed in critical electronic components, precise models for active and passive devices, and demonstrators needed for the aforementioned applications. This will enable the mass production in Europe of electronic circuits for these applications and help to keep and grow the European development and engineering knowhow on advanced technology devices and circuit concepts and designs.

The three MMW/THz technology platforms focused on in this project highlighted:

- The integration and optimisation of the SiGe HBT and back-end modules developed in previous projects (FP7 DOTFIVE and MEDEA+ SIAM) into a new advanced core CMOS technology (55nm) in order to obtain a 0.5THz 55nm SiGe BiCMOS platform suited for RF, MMW and THz SOC applications;
- An integral approach, focusing on improvements and breakthroughs with respect to previous BiCMOS technology generations of the essential high performance passive RF components. The RF packaging and the required RF testing solutions have also been part of this technology development framework. The work in this module has been based on, and validated using, the newest SiGe BiCMOS technology;
- The development of silicon photonics devices for future silicon photonics foundry offerings. The work in this module has been based on, and validated using, IHP SiGe BiCMOS technology, and has been conducted with the objective of possible integration in the 0.5THz 55nm SiGe BiCMOS technology.

Ready for the taking

These technology platforms are now available in Europe for prototyping and production. Demonstrators have been developed to show potential of all three platforms for growing MMW and THz markets. These markets used to be based on so-called III-V semiconductor technologies, and therefore limited by high manufacturing costs, high power-consumption and the limited integration scale of associated technologies. Importantly, all this is changing rapidly, with silicon now being considered as the semiconductor material of choice to address such applications, thanks to the high innovation level of the project results.

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Health and aging society
- Safety and security
- Design technology
- Process development
- More than Moore

PARTNERS

Advanced System Developments and User Services / Agilent Technologies / Alcatel Lucent (Now NOKIA) / Astra SES / Robert Bosch
Bruco Integrated Circuits / CEA-LETI
ENSICAEN / ESIEE Paris / Fraunhofer Institute / Grenoble Institute of Technology
IEMN / IES / IHP / IMS
MASER Engineering / Micram Microelectronic
NEWTEC / NXP Semiconductors
Salland Engineering / Silicon Radar
STMicroelectronics / SynView
Telecom Bretagne / TU Berlin
TU Delft / TU Dresden
TU Eindhoven / Uni Saarland
Uni Siegen / XMOD Technologies

COUNTRIES INVOLVED

- Belgium
- France
- Germany
- Luxembourg
- The Netherlands

PROJECT LEADER

Jean-Louis Carbonero
STMicroelectronics

KEY PROJECT DATES

July 2011 - December 2015

Today, there are production projects involving BiCMOS55 customers, on fibre optics communications up to 100Gb/s; 77GHz automotive radar; and high speed instrumentation. One customer is already in production of several circuits addressing 100Gb/s communications; and seven customers are at prototyping level for circuits covering the other applications.

In addition, the BiCMOS55 55nm technology platform, including its PDK, is also available to all circuit designers; and new customers can use this technology for their product development.

As a side note, most of the circuits produced by the project achieved very high performance levels, making Europe a leader in the field of MMW and THz.

This project involved 33 partners, from Belgium, France, Germany, and The Netherlands, and represented an effort of 235 person-years. Strong cooperation and interaction among project partners lead to its success. It also generated more than 240 international publications – mostly co-authored by one or more partners – and played a part in international conferences.

New services, opportunities and momentum

Importantly, RF2THZ created new market opportunities. It achieved this by offering:

- New services at a reasonable cost;
- Highly integrated solutions for wireless multi-gigabit data rate transmission;
- New capabilities for the transportation and security sectors;
- Intelligence in building control based on radar sensors;
- Introducing the worldwide most advanced high speed D/A-converter platform.

Thanks to RF2THZ, industry is also expected to generally benefit in the medium term from new application areas and revenue streams. In developing and demonstrating industry-standard, silicon-technology platforms for a number of promising application domains, it provided project partners with excellent opportunities to address technological challenges in this innovative field cooperatively, and to move up the learning curve. For example, designing integrated circuits for MMW and THz applications requires a different approach and methodology and set of tools. However, the experience gained from designing the demonstrators gives project partners a competitive advantage in developing future products in the MMW and THz application domain.

Significantly, the supply of silicon technology-platforms able to handle greater than 100 Gbit/s optical communications to serve the requirements of ultra-high speed communications will give momentum to European chipmakers and the telecommunications industry. These platforms are essential for the evolution of future high-speed communication products.

In addition to technical, commercial and financial advantages, RF2THZ also delivers societal, environmental and security benefits. Development of 77/120 GHz radar sensors for automotive applications will boost road safety by enabling development of new driving aids such as MMW radar. Advanced SiGe BiCMOS technologies make automotive radar affordable for all price segments and hence to the broad society. Other applications include passive MMW imaging technologies for improved airport security, and intelligent building controls to reduce energy consumption, while providing enhanced user comfort. Demonstrators targeted automotive applications with very stringent quality requirements so that these technology platforms can serve as industry standards for such products.

Supporting a fundamental building block

In a nutshell, the RF2THZ project strengthens Europe's electronics business and competitive-edge by supporting research and development in key silicon technologies and applications; it is also likely to contribute towards improving Europe's society and economic climate by the leveraging effect which is inherent to microelectronic technologies. After all, the semiconductor industry is a fundamental building block of the new economy.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

PROJECT RESULTS

CT305 | Towards reducing 450 mm wafer production costs by 30% and improving European competiveness [SOI450]

The SOI450 project aims to develop silicon-on-insulator (SOI) substrates for the transition to 450 mm silicon wafers. It is expected to stimulate European infrastructure to take a lead in this and related work, in order to ensure Europe will be fully-prepared to participate and contribute actively to the wafer-size transition in this innovative and technology-driven market segment. Although this project was halted temporarily in mid-2014, it did have several key achievements.

Silicon-on-insulator (SOI) is an innovative way in chip fabrication for replacing bulk silicon wafers with multilayer ones. These SOI substrates are strategically used in the transition to 450 mm wafers in order to meet cost per transistor requirements, and be able to continue to exploit Moore's famous law. By increasing the wafer surface by a factor of 2.25, the 450 mm wafer is expected to reduce production costs by 30%, compared to the 300 mm.

Notably, the transition to 450 mm manufacturing means huge efforts and total alignment with future standards. However, this can only occur (at the right time) when many important and significant factors come together, including a:

- Compelling manufacturing return on investment;
- Strong supplier readiness;
- Critical mass of device makers who need to make the transition.

Gearing up for a successful 450 mm transition

The SOI450 project started in November 2011. The goal was to bring 450 mm SOI and related technologies to an appropriate maturity for a 450 mm transition in the middle of the decade, with the first dies on 450 mm expected around 2015.

To reach this goal, a consortium of eight partners from four European countries provided access to expertise and other resources in market leading silicon research, design and fabrication, as well as, to a supply of equipment and process solutions linked to SOI substrates production.

The project was divided into three work packages:

1. Management, roadmap alignment, targets and assessment;
2. Specific-equipment design & development;
3. SOI processing implementation

Following the alignment and technical maturity assessment phase, some important project work was done and key tools delivered. In particular, cleaning solutions were developed on an EVG bonding tool using megasonic cleaning (a type of acoustic ultrasonic cleaning). In addition, the Adixen Pod Analyzer (APA) was deployed in the 300 mm fully-depleted silicon-on-insulator (FDSOI) substrate line. This will improve yield and optimise FOUP (a specialised plastic enclosure to hold silicon wafers securely and safely) in cleaning costs. The final design of the SOI bonded system was also achieved and validated. Crucially, the bonding quality of the cleaning module and the IR inspection reached the specification targets for 450 mm.

Furthermore, the research & development inspection platform is also available. The software and data management system was updated to be compatible with wafer size, resolution needs and higher volume of exchanged data. Finally, the complete SOI process was demonstrated and validated, all process steps tested and the bonding tool installed and produced excellent cleaning / bonding results;

In terms of prototypes. Altatech developed the table-top 450mm metrology system, Altasight, which can interface with major players in material and process developments. And Adixen's study and assembly of its APA450 prototype, and its installation at G450C (Albany, USA), gives the company a forefront position in the area of molecular contamination, and an big advantage with international customers.

Unfortunately, the SOI450 consortium decided to halt the project temporarily in June 2014, at the behest of the project co-ordinator (Soitec). This was due to doubts expressed by integrated device manufacturers about the then-market for the 450 mm, which was followed by subsequent delays in the project roadmap, and inherent economic and technical consequences.

PROJECT CONTRIBUTES TO

- ✓ Energy efficiency
- ✓ Design technology
- ✓ Process development
- ✓ Manufacturing science
- ✓ More than Moore
- ✓ More Moore

Technology node / 22 nm

PARTNERS

INTEL PLS`
EVG
ALTATECH
ADIXEN
ASM
LETI
IMEC
SOITEC

COUNTRIES INVOLVED

- Austria
- Belgium
- Ireland
- France

PROJECT LEADER

François Brunier
SOITEC

KEY PROJECT DATES

November 2011 - December 2014
(temporary)

Perfect poised to restart

On a positive note, the consortium will be ideally positioned when SOI450 is finally restarted, and for several reasons. The project has achieved a level of maturity in SOI 450 mm technologies and equipment. Furthermore, what has been technically demonstrated with the 450 mm is mostly 'retrofitable' in the 300 mm; and project partnerships increase sharply the value of these developments. Crucially, Soitec remains connected, through the SOI450 project, to the G450C (the global consortium focused on building the 450 mm wafer and equipment development environment).

Technical and technological triumph

Now, there are very good reasons why this project should be completed. On the technical and technological side, SOI450 will ensure the fabrication of SOI substrates at the right moment for time to market. SOI will deliver a powerful tool to balance power efficiency and performance: it provides increased transistor switching speed of more than 30%, power reductions of 50% or a trade-off in lower/performance and superior isolation for circuit and design. It also enables compact integration of intellectual property (IP) blocks. Furthermore, SOI will play a key role in the 'more Moore' race as it responds to most of the scaling challenges. These ultimate nodes are the ones targeted by 450 mm transition.

Good for European business and competiveness

SOI450 also involves the development of equipment and materials for the next generation of semiconductor devices, and new business opportunities. These products define a huge, self- sustaining market by themselves. In these global markets, the European equipment and materials industry has achieved a world-leading position and acts as a powerful European engine for economic growth in its own right.

The introduction of the 450 mm wafer diameter will be a new opportunity for the European equipments and materials industry to improve its competitiveness and gain market share.

A case in point is Soitec. This European manufacturer produces 80% of SOI substrates and is the global leader in this field. As SOI substrates are one key path to nanoscale CMOS – identified by end users for digital applications, system-on-chip devices and memories – large volume applications are forecasted, deploying possibly the 450 mm. It is therefore essential to capture this market with the transition to 450 mm.

The project also aims to stimulate the European infrastructure concerned with 450 mm development on SOI materials and related advanced technologies, such as bonding, cleaning and thermal treatment. The objective is to increase European leadership and competitiveness within this highly innovative and technology-driven market segment. This target requires a joint effort for the development of innovative substrates and equipment.

Now, SOI 450, together with other European 450 mm projects, will have a significant impact on further R&D activities. It will provide access for the companies involved and European research institutes to the necessary 450 mm SOI technology. Without European and national funding, worldwide co-operation and the access to 450 mm would be very limited because a large part of the development work would then be performed in Asia or the USA.

Finally, such projects are an important way for the European equipment and materials industry to participate in next-generation wafer technology, and in the worldwide market for 450 mm equipment and materials. It is envisaged that, because of their huge size, there will only be a small number of 450 mm high volume fabrication facilities built around the world. It is therefore very important that Europe ensures that at least one such facility is built and operated in the region.

CATRENE Office
9 Avenue René Coty
F-75014 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

Cluster for Application and Technology Research in Europe on NanoElectronics

CT306 | Standards-compliant tools for 450mm production reinforces European semiconductor industry's position (NGC450)

The NGC450 project successfully delivered the necessary means to re-tool production lines to migrate from 300mm to 450mm wafer production, while still adhering to international standards and keeping costs down.

Common software and robotics platform drives 450mm wafer development & production

The move by leading chipmakers to abandon 300mm wafer production in favour of the larger 450mm ones will improve production volume and the yield of viable devices. There was, however, an initial downside: new equipment was needed to handle and process the larger wafers, resulting in much increased investment costs to build a semiconductor fabrication plant (commonly called a fab). In addition, such a transition required considerable research and development (R&D) effort and presented substantial technical and financial challenges.

Innovative and promising

The NGC450 project aimed at helping Europe develop a wafer-handling platform, dedicated to supporting the 450mm wafer size migration. The project was conducted in two phases: development of a wafer-handling R&D platform; followed by integration into a fab environment to assess its throughput versus a 300mm benchmark, involving the simulation of wafer processing times. All development work was compliant with the International SEMATECH Manufacturing Initiative (ISMI) standards and specifications.

NGC450's key achievements and deliverables can be summarised as follows:

- Atmospheric equipment front-end module with preliminary equipment for automated wafer-loading was developed, and a detailed state-of-the-art unit assembled for final characterisation The challenge was in transferring heavier substrates through a longer distance within an equal period of time, despite increased vibrations phenomenon and more challenging mechanical properties of the substrate. Atmospheric robotics were able to maintain the same throughput as a 300mm system, with optimal wafer safety and extreme cleanliness;
- Vacuum robot and a linear vacuum chamber, as well as, vibration-free, stiff and very thin end-effectors for atmospheric and vacuum environments were developed. The end-effectors fully comply with low defectivity, safe-handling efficiency and contamination (particle and metallic) demands. Viability to produce an easily scalable vacuum chamber while maintaining the same throughput as a 300mm cluster system was successfully tested;
- Compliance with 16-22nm cleanliness and airborne molecular contamination was proven. The efficiency and stability of the software to drive a multi-equipment cluster with a high-performance interface was tested;
- The project implemented specific vapour phase decomposition (VPD) and liquid phase decomposition (LPD) set-ups on 450mm wafer and optimised metallic contaminants collection coupled to the advanced inductively coupled plasma mass spectrometry (ICPMS) characterisations. The set-ups' efficiency and sensitivity were fully tested to characterise the contamination levels of the robotics;

CT306 | **Standards-compliant tools for 450mm production reinforces European semiconductor industry's position** (NGC450)

Partners:

AIS
ASYS
CEA-LETI
EVG
Fraunhofer
HAP
Intel
RECIF

Project leader:

Guilhem Delpu
RECIF Technologies

Key project dates:

Start: November 2011
End: December 2014

Countries involved:

Austria
France
Germany
Ireland

PROJECT CONTRIBUTES TO

Communication	
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	✔
Manufacturing science	✔
More than Moore	
More Moore	✔
Technology node	<22nm

- Specifications of the robotics and software to ensure compatibility between the wafer-handling platforms developed within this and other current projects;
- Specification review of cleanroom space and the logistics and fluids needed for the tools;
- Development, review and assessment of specifications necessary to support a silicon-on-insulator (SOI) production line.

Beneficial European collaboration

Crucially, NGC450 has helped to mitigate the technical and financial challenges that 450mm migration raises, as far as wafer handling and automation are concerned. This will help the European semiconductor materials and equipment industry to optimise R&D efforts and minimise related risks. The ultimate objective of NGC450 and its eight project partners from four European countries was to build a comprehensive package that will address 450mm challenges by allowing European companies to focus on a common target and share the same hardware and software interfaces. The development around a common software and robotics platform will share key skills and the risks, limit redundant development in robotics and automation and thereby limit overall R&D costs.

And the results are promising. According to one consortium member, this project delivered off-the-shelf, turnkey automation with fast throughput. All of this will help reduce the time to market for European-made 450mm enabling technologies and offer interoperability advantage to European equipment suppliers. It will also consolidate the European semiconductor equipment industry's global leadership position, with project partners expected to secure European competitiveness in the promising 450mm market.

Furthermore, a significant part of the R&D output will be dedicated to the improvement of current 300mm applications targeting the sub-20nm technology node and focusing on cleanliness, throughput and yield improvement. This is, therefore, also an opportunity to sustain the European semiconductor industry in the existing 300mm market.

European and global sales opportunities

Equally important is the non-European market where European semiconductor production equipment and materials companies tend to score bigger sales. In fact, one project partner has secured more than a 25 percent share of the worldwide market in 300mm wafer sorters over the last decade. More than 90 percent of its turnover now comes from outside Europe (Europe accounts for only seven percent of its worldwide installed base of nearly 700 units of 300mm equipment). NGC450 also presents valuable opportunities for Europe to establish and develop its own share of this global market, where American and Japanese equipment suppliers are already well established in this new 450mm segment. By providing these European enterprises the chance to co-operate to optimise R&D efforts and minimise related risks, this project helped reduce their time to market and provided them with an interoperability advantage.

Consistent, uniform and economical

NGC450 used the findings and results from the first ENIAC 450mm project (EEMI450 project). It will now act as a reference for subsequent 450mm projects. In the same way, some of NGC450's output will now be used by other related projects, like ENIAC EEM450PR, ensuring consistency and uniformity with preceding and subsequent projects which are part of the EEMI450 initiative. Importantly, it will also mean making excellent use of work already done, thus reducing project time, effort and costs.

CATRENE Cluster for Application and Technology Research in Europe on NanoElectronics

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

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CT402 | Crucial ambient intelligence elements in place for consumer and healthcare applications [9D-Sense]

The smart wristlet illustrates a truly winning application of ambient intelligence

The 9D-Sense project developed and tested state of the art technologies suitable for installation in an autonomous sensing module that integrates key sensor elements in a single device. This development is crucial to ambient intelligence and the market for cost-competitive solutions in consumer and healthcare electronics. It also helps maintain European dominance in this global market.
Key to the 9D-Sense project and at the very heart of ambient intelligence is the ability to sense an object's physical movement in different directions – hence the so-called nine degrees of freedom or 9D for short – such as gesturing. The 9D sensing module developed in this project embraced key technologies crucial to fabricating micro-electrical sensors, efficient energy harvesting and storage, and secure wireless communications.

Crucial technologies, algorithms and applications

The main goal of the 9D-Sense project consortium, comprising seven technology concerns and two universities, from three European countries, was to provide novel processing technologies and innovative methods to produce a stand-alone 9D system. It was based on a three-axis accelerometer, three-axis gyroscope and three-axis magnetometer, and needed to communicate through a secure data-transmission protocol. These requirements were in response to application and market demands for small sensing modules with low-power consumption, a self-sustaining power supply and secure data transfer.

In particular, these demands called for the development of a wide range of semiconductor technologies for MEMS (microelectromechanical system) sensors (like on-chip integration), ASIC (application-specific integrated circuit) processes for high-capacity micro batteries, as well as, application-specific algorithms with protocols for secure data transfer. Furthermore, energy harvesters (which generate and provide enough energy to feed the system electrically) were also needed.

9D-Sense developed the following:

- Technologies for integration of micro sensors on a single chip and technologies for smaller package size;
- Technologies and processes for a thin film battery;
- Two types of energy harvesters – kinetic and thermos-electrical generator – capable of converting kinetic and thermal energy into electric energy;
- Efficient power management;
- Algorithms for specific applications;
- Secure communication framework for internet of things.

In addition, this project validated algorithms and secure communications in the 9D sensing module in three different use cases:

- Pedestrian Tracker: used to track a person's movements and path travelled, and graphically display them in real-time on a mobile device;
- Orthese Knee Control: used to track and control the movement of a type of prosthetic electronic knee joint;
- Smart Wristlet: a communicating, wearable device that manages access rights by recognising gestures of the wearer, and securely transmitting them to the internet of things.

Ideally suited healthcare and consumer applications

What we now have are key elements that will be integrated in ambient-intelligent applications. These elements are highly autonomous, energy-efficient, ultra-low-powered sensing systems which are found in 9D-Sense's two focus application areas with societal impact – medical/healthcare and consumer – where substantial demand and large market volumes are expected.

Healthcare and monitoring applications range from prosthetics/orthopaedic appliances and ambient-assisted living for the elderly and disabled, to joint-monitoring (such as orthopaedic knee braces for the disabled) and monitoring during patient rehabilitation.

There are other novel applications. Ambient intelli-

Partners:

Robert Bosch
Bosch Sensortec
Fraunhofer
Gemalto
HSG-IMIT
Micropelt
Otto Bock HC
TU Darmstadt
University of Helsinki

Project leader:

Ricardo Zamora
Robert Bosch

Key project dates:

Start: November 2011
End: October 2014

Countries involved:

Finland
France
Germany

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	✔
Safety and security	✔
Energy efficiency	
Digital lifestyle	
Design technology	✔
Sensors and actuators	✔
Process development	
Manufacturing science	✔
More than Moore	✔
More Moore	
Technology node	<130nm

gence can also be applied to positioning or navigational devices for use indoors (where global positioning systems do not work); and in security or home automation, such as intrusion detection by movement, or control and condition monitoring in buildings for improving energy efficiency.

Strengthening European manufacturing and research

The focus areas addressed and investigated in 9D-Sense contribute to several initiatives of the European Union as well as to strengthening the market position of European manufacturers and researchers.

MEMS sensor production for non-automotive applications, for instance, is still an important business case for European companies. Notably, the demand for integrated sensors (so-called combos) is expected to grow in the coming years and will partly replace discrete sensors. Unlike many other semiconductor-based technologies, two key players among dominating suppliers are located in Europe.

Crucially, since most consumer-electronics manufacturing takes place outside Europe, it is important not to lose ground in the remaining enabling technologies. MEMS sensors and actuators – such as inertial, pressure, humidity and geo-magnetic sensors, and micro-mirrors for display applications – are meanwhile critical elements users expect in their mobile computing-devices. Recent market-share losses to players outside Europe need to be regained, and the overall market share has to increase to a leading position in order to leverage volume-scale effects.

Thanks to this project, European-produced inertial sensors are now available for innovative, future markets, like communication or healthcare, thereby strengthening the position of European companies in the field of MEMS technologies and products. This also means supporting a European effort in maintaining its leadership in more-than-Moore technologies, together with technologies for heterogeneous integration and smart manufacturing. Furthermore, providers of systems using 9D sensors (such as internet of things or medical/health care applications) also benefit from 9D-Sense.

A case of success

The market for wearable devices is an important and rising one, but largely immature. Major issues still need to be resolved before it can reach its full potential:

- Connectivity: there is a lot of heterogeneity in the communication protocols today; no clear standard has emerged yet;
- Ergonomics: wearable objects are too small; efficient interaction schemes still have to be defined and need to be easy to use in everyday activities;
- Autonomy: users already have a lot of devices to keep charged every day; adding more of these devices will quickly become a big issue;
- Design: wearable devices are very personal, and their design very important to users;
- Security: the more control we relinquish to these devices, the more they become security weak-points; therefore good security must be built into these devices;
- Privacy: as personal objects, wearable devices are inherently gateways to personal activity-tracking.

That is why the Smart Wristlet is so remarkable. A by-product of this project (it was developed as a demonstrator), this innovative wearable device has excellent commercial potential. Notably, it also deals successfully with all the issues previously mentioned. In addition, it allows for seamless integration into existing systems; its protocol framework is built to be battery-friendly and independent of transport protocols; and it fully deploys power harvesting and thin film battery solutions delivered by 9D-Sense.

Even though there is still some work to be done before the Smart Wristlet is ready for the marketplace, the technical solutions it demonstrates could be integrated today in other products. More importantly, it sums up and embodies everything 9D-Sense set out to achieve.

CATRENE Cluster for Application and Technology Research in Europe on NanoElectronics

CATRENE Office
9 Avenue René Coty - F-75014 Paris - France
T. +33 1 40 64 45 60
E. catrene@catrene.org
www.catrene.org

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CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

CALL 4

PROJECT RESULTS

CA109

Hybrid architecture, many-core TSAR processor and algorithm parallelisation feature in new high performance computer [SHARP]

The SHARP project played a significant role in investigating and prototyping a new high-performance computer (HPC) hybrid architecture – an extension of the existing BullX HPC system – and in the design of the many-core TSAR processor in 2.5D silicon technology. On the application front, SHARP addressed algorithm parallelisation and the porting of existing sequential code to the hybrid HPC architecture.

Performance in scientific computing (measured in 'flops' or floating-point operations per second) has increased significantly: from teraflops in 1997, to petaflops by 2008. Industry and market demands are now driving exascale systems (a thousand-fold increase over the first petascale computer), when the number of processing cores is also expected to increase dramatically. Many countries world-wide are investing in high-performance computers (HPCs) to maintain their key positions on the world stage in diverse industrial sectors.

Indeed, Europe needed to invest in HPCs to model and simulate the scientific advancements required to develop its future products and services. It was quite clear that economies that make such an investment are those that will, over time, gain the greatest competitive advantage and reap the largest economic benefits. Hence the current scramble to invest in large-scale leading-edge HPC systems world-wide.

This was the technical and technology backdrop and business case that triggered the SHARP project in 2012, and guided it to its completion in 2015.

Focus on performance, power consumption and scalability

SHARP is based on the premise that the future of high performance computing lies in heterogeneous and massively parallel computer systems that can support efficiently the large spectrum of (potential) applications. This highlights the ever-increasing need for performance, with efficient power consumption a close second. This project set out to create a generic and flexible HPC architecture based on key considerations – performance, power consumption and scalability, together with reliability, flexibility, heterogeneity and security. Developments in SHARP addressed not only hardware and software (especially programmability) aspects, but also application implementation for the purpose of validation and demonstration.

In order to compare against the state-of-the-art, SHARP used the Top500 classification of supercomputing. This is based on a recent high performance conjugate gradient (HPCG) criterion (to balance floating point processing, communication bandwidth and latency with a focus on messaging, memory and parallelisation) which provides a new classification of existing HPC solutions.

Major technical achievements and deliverables include:

- Design and prototyping of a generic HPC architecture integrating a variety of computing technologies (many-core CPU, GPGPU, FPGA);
- Complete design of the TSAR processor in a 2.5D silicon technology (tape-out);
- Software development (OS, specific application layers, etc.) in relation to various computing technologies, and to support security features;
- Optimal implementation of a large range of applications on heterogeneous computing technologies: Examples include video processing (multi-core CPU+FPGA); traffic light recognition (many-core CPUs); medical image processing (CPU+GPU); and system prototyping (CPU+FPGA).

Collaborating closely with Europe

The five-member European project consortium had wide expertise and experience, ranging from hardware development for open servers and HPC solutions, heterogeneous systems design and analysis, to parallelisation and embedded solutions dealing with telecom, multimedia and security applications.

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Health and aging society
- Safety and security
- Energy efficiency
- Digital lifestyle
- Design technology
- Technology node

PARTNERS

Bull
Thales Communications
CEA/Leti France
UPMC/Lip6
FZI

COUNTRIES INVOLVED

France
Germany

PROJECT LEADER

Huy-Nam Nguyen
Bull

KEY PROJECT DATES

September 2012 - August 2015

Co-operation between SHARP partners was excellent due to the fact that the core consortium had worked together previously on past projects. There were also links with other European and national projects which, for instance, provided funding for the silicon design of the TSAR processor. SHARP also worked with other external partners, like CEA/Dam and UPEC, in such specialist areas as eG and medical image processing, as well as in implementing the proprietary QPI protocol on the field-programmable gate array (FPGA). The latter it did in close collaboration with Intel and Altera.

On the promotion, information sharing and innovation front, three patents were filed; four PhD theses, based on the work done in SHARP, were successfully defended; and 18 technical papers were published.

The drive to invest in HPC

SHARP's deliverables provide European industry with the means of securing and maintaining its competitive edge. Thanks to its HPC solution, this project will enhance computing performance in a very large range of applications – from complex system modelling and simulation, to real-time data mining and image processing. This allows industry to maintain its key position on the world stage in sectors as diverse as automotive, pharmaceuticals and financials, as well as, biological and renewable-energy. It also provides industry with the drive to invest, or continue to invest, in HPC: it is the only way to model and simulate the scientific advancements needed to develop future products and services.

The rewards also look promising. The global high-performance computing market is projected to reach US$ 36.62 billion by 2020, at a CAGR of 5.45%. The emergence of big data has also increased the demand for HPC clusters to handle a data-intensive workload and support high-performance simulation and data analysis. Equally encouraging, the cloud-related HPC market is estimated to grow from US$ 4.37 billion in 2015 to US$ 10.83 billion by 2020, at a compound annual growth rate (CAGR) of 19.9% from 2015 to 2020.

Going the extra mile

Unusually, many of SHARP's developments go far beyond their initial objectives, such as finding and applying solutions, like HPC components, to real-life industrial problems, and exploiting prototypes, tools, methodologies and educational materials in industry. This illustrates and reflects the drive of the project partners and the efficiency and effectiveness of the project results.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

PROJECT RESULTS

CA110 | Advanced STB delivers 'Smart Home' functionality and flexibility

[AppsGate]

The AppsGate project draws on the broad expertise and experience of prominent European actors for the purpose of developing and demonstrating advanced set-top boxes (STBs). These are primary, point-of-entry devices that offer homes a variety of digital applications targeted typically at residential automation, energy management and healthcare. These are integrated seamlessly with legacy STB services, and delivered in a flexible, user-friendly fashion, thanks to an innovative residential gateway.

AppsGate was conceived at a time when service and content providers and technology companies were keen on enhancing their offerings to the residential consumer. There were also other drivers at the time. Set-top boxes (STBs), the primary point of entry of services into the home, were capable of a lot more than media services. Thanks to their (affordable) computing power and functionality, as well as, the availability of open-software frameworks and connectivity standards, a new world of integrated home services could be created.

The project consortium, comprising prominent European electronic chip suppliers, consumer electronics OEMs (original equipment manufacturers) and service providers, were charged with developing and demonstrating advanced STBs and related products that support such features as, home automation, energy management and healthcare applications, and which seamlessly integrate with legacy STB services.

Stacking the deck

Project objectives were to develop, validate and deliver the three 'pillars' of the AppsGate platform: multimedia home gateways; Android STPs; and smart home solutions. There were challenges right at the start of the project, when the consortium quickly realised that no single software framework was available to address all project demands and requirements. A software stack was therefore devised to provide the most appropriate solution for broadcast, broadband and the smart home, at the expense of some integration complexity.

The project encountered several problems which it successfully resolved as follows:

- Broadcasting: solved using STB 'middleware' (a general term for software that serves to bridge already existing computer programs), designed to provide the best quality TV services by using multimedia hardware features embedded into STB chips;
- Broadband: handled by the Android operating system which provides instant access to countless apps and over-the-top content (OTT) services, and which offers a framework for monetising new ones;
- Smart home: posed a unique set of challenges. The system had to be capable of identifying new services, adapt to devices coming and going, manage diverse communication protocols, and exchange information and services. In the absence of any widely adopted standard, AppsGate took two complementary approaches based on technologies available from the consortium partners. The first one was designed around the message bus; and the second approach implemented a service broker using an 'application abstract machine' (ApAM).
- End-to-end security and data privacy: handled using technology developed to protect premium content in STBs;
- Usability: considered early on because it drives system acceptance. Natural language was, for instance, deployed by end-users for specifying home automation scenarios;
- Integration of a deep technology stack with a large number of interfaces: addressed using 'clusters' of experienced and expert project partners formed around each hardware platform. This concept of a 'collaboration cluster' proved very effective by making interactions simpler. It also enabled tighter integration of partner technologies than initially planned, and sparked new ideas that were readily implemented.

All deliverables were on time and the goal of bringing an open platform that could deliver new home services was achieved, given the wide spectrum covered by the applications actually demonstrated.

AppsGate is technically elegant for several reasons. By leveraging the multimedia strengths of the STB, it enables home services to be seamlessly integrated and accessible from a single, unified interface, thus offering convenience, and reducing the costs of new services by sharing hardware and broadband connection. And speed is of the essence. An open platform will deal with a fast-changing,

PROJECT CONTRIBUTES TO

- Communication
- Health and aging society
- Safety and security
- Energy efficiency
- Digital lifestyle

PARTNERS

STMicroelectronics
Pace
Technicolor
NXP
4MOD Technology
ARD
Immotronic
Ripple Motion
Simon Tech
Video Stream Network
SoftKinetic Software
Softkinetic Sensors
University UJF/LIG
Institut Mines-Telecom

COUNTRIES INVOLVED

- France
- Spain
- Belgium

PROJECT LEADER

Jean-Christophe Pont
STMicroelectronics

KEY PROJECT DATES

September 2012 - February 2015

dynamic market where operators and service providers must deploy new services quickly to lure new customers and counter competition.

Furthermore, extensibility allows users to install services and devices gradually, starting with a basic configuration and later extending it as experience and confidence grows. And not forgetting the end-user, key to the adoption of advanced home services is an intuitive, contextual interface suited to all user types, especially the less technology-literate, elderly and physically impaired.

Heading for the marketplace

The first products based on AppsGate technologies have already reached the market. The most notable of these is the Cube S of Canal+ developed by Technicolor around ST's system-on-chip; followed by more Android STBs from Technicolor and Pace. ST has also secured customers for the cable gateway bundled with NXP's Full-spectrum Transceiver. Furthermore, 4MOD is shipping the BLE remote control and the 6LoWPAN is under evaluation with huge volume prospects.

In addition, Simon Tech unveiled a new line-up of Z-Wave products; ARD, Immotronic, SoftKinetic and VSN made use of their project expertise to strengthen their product roadmap. And AppsGate's Smart Home, installed in INRIA's Rhône-Alpes living lab, is being used for further research.

Everyone's a winner

Far-reaching, AppsGate will impact end-users and industry, together with society in general. Not far-fetched, however, it could easily provide effective support to the European effort to handle an ageing population by controlling healthcare costs, improving energy usage and providing high-quality interactive entertainment to every home.

There are also significant benefits to a wide range of stakeholders. End-users are expected to be the main recipients of AppsGate services. These services will bring to many an opportunity to access information and to use the Internet for a wide variety of activities. It may even entice Europeans without an internet connection today to acquire one, thus helping to further bridge the digital divide. And service providers can offer multiple services, such as home control/monitoring, without using incremental capital.

And there is more. Medical care-providers can offer high-quality care to an increasing number of patients using limited financial and human resources. Furthermore, moving patient care from the hospital to the home is expected to result in cost-reduction and improved quality of life. On the electronics side, AppsGate will allow European chip suppliers to stay at the forefront of integration, with nearly one billion transistors in a single system-on-chip (SOC), and their capability to deliver a complete and compact solution comprising a system-in-package (SIP), software stack and reference board.

There are also other benefits. Networking technologies, for example, provide full home-coverage with no additional wiring; the number of 'boxes' is reduced along with their complexity; and content in many formats and from multiple sources is processed through a single, consolidated and adaptive interface. This convergence process is creating opportunities for European industry; but what's more, new applications will drive consumer behaviour, which in turn will generate new revenue streams. Certainly a winning solution.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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PROJECT RESULTS

CA111 | Launch of Ultra-High Definition TV expected by 2018 and mass rollout by 2020

[UltraHD-4U]

Ultra-high definition TV (UHDTV), synonymous with digital-cinema quality in the home, brings a full cinematic experience to residential viewers. With this attractive consumer offering in mind, the UltraHD-4U project and its project consortium, comprising partners from across the value chain – from content creation and home displays, to integrated-circuit vendors and academics active in standardisation – researched and developed the necessary elements needed to make UHDTV a reality.

Television viewers with their high-resolution flat-screen TVs are just getting used to the clarity and detail of high-definition (HD) television. However, hardware and content suppliers continue to delight and entice consumers with greater higher levels of 'immersiveness' through increasingly better TV reception and resolution (higher number of pixels), especially for screens that are 50-inches and larger. Hence the attraction for ultra-high definition TV (UHDTV), also called 4K.

Delivering an immersive TV experience

The UltraHD-4U project aimed at studying and setting up an end-to-end 4K UHDTV chain (broadband and/or broadcast) for use residentially by consumers and at dedicated show-points. This is commercial quality, audio-visual content normally found in a 'digital' theatre equipped with the latest 4K-rendering and broadband-communication technologies for receiving and processing high-resolution, high-quality digital content. A fast-moving state-of-the-art drove the project to promptly address most of the functions around real-time UHD Main10. Importantly, this also includes 'high dynamic range' (HDR), a video technique that heightens a picture's dynamic range – the contrast between the brightest whites and the darkest blacks – and 'wide colour gamut' (WCG), a colour space that offers a wide colour range by using pure spectral primary colours.

Main project activities included investigating, developing or implementing the following key components and features:

- System architecture for UHDTV;
- High-efficiency video coding codecs (a codec is hardware or computer code capable of encoding or decoding a digital data stream or signal);
- Advanced features, such as deep colour, colour space and resolution, high dynamic range, higher frame-rate and high-speed connectivity;
- A new, high-bit-rate, high-definition multimedia interface (or HDMI, an all-digital audio/video interface between a set-top box or DVD player, and a digital TV set, for example);
- Interoperability and backward compatibility with deployed HDTV infrastructure, required distribution bandwidth and audio;
- UHDTV-frame-compatible 3DTV with a display technology that works with or without special glasses;
- UHD in professional applications, such as medical and display;
- Use cases and five demonstrators, together with experiments to assess different aspects of the demonstrators.

A well-equipped project consortium

The UltraHD-4U project consortium took into account digital TV's fast technological pace, as well as its own keen desire to involve leading European field-experts to participate and contribute to a common vision on UHDTV's evolution. This called for a considerable amount of commitment, organisation and expertise. Appropriately, partners range from creators of content for home consumption, and academics active in the standardisation, to global leaders in the manufacturing and distribution of chips, encoding devices, set-top box and displays.

Project partners also played a significant role in major standardisation bodies, technical forums and trade shows, with more 180 public presentations and articles. In addition, more than 14 UHD-related product prototypes or technologies were developed, underscoring the huge impact UltraHD-4U has on project partners as they expand their intellectual property rights' (IPR) portfolio while ensuring they are well-prepared for market ramp-up.

Focus, synergies and infrastructure

UltraHD-4U provides novel possibilities for industry, as well as, public and private research institutions. Importantly, collaboration between partners and specialists ensures a much deeper and comprehensive approach. The development of new content formats, and capture, coding and rendering technologies, together with IC's used in consumer devices, will be crucial to industry partners, content producers and distributors

PROJECT CONTRIBUTES TO

- Communication
- Energy efficiency
- Digital lifestyle
- Design technology

PARTNERS

Alioscopy
Arçelik
ARTE
Barco
Binocle
Hispasat
mediAVentures
Pace (now ARRIS)
RTVE
Sapec
STM
Technicolor Connected Home Rennes (TCHR)
Technicolor R&D France (TRDF)
Thomson Video Networks (now Harmonic)
University of Nantes/IRCCyN
Vitec

COUNTRIES INVOLVED

- Belgium
- France
- Spain
- Turkey

PROJECT LEADER

Issa Rakhodai
Pace France

KEY PROJECT DATES

April 1, 2013 - March 30, 2016

in maintaining Europe's position beyond the HDTV transition. They will also play an important role in preparing and expediting European and worldwide deployment of UHDTV. This project is expected to create focus and synergies between consortium partners, enabling European contributions to solutions in the way of components and systems, but also user benefits and business models.

This project will also help reduce implementation time by ensuring that at least part of the chain is ready to be integrated, while providing European universities and other research institutions with opportunities to establish the right level and quality of research in the field of networked media that will be really crucial to Europe in a global context.

The new infrastructure will help to further expand research and training at universities in the field of UHD media technologies. Moreover, this project will enable research institutions to valorise elements of their research, both directly (via technology licensing) or indirectly (via spin-off ventures), thus accelerating the required technology transfer.

Energy conscious

When defining HDR and WCG, the project paid particular attention to energy-saving. For instance, the MaxFALL (frame average light level) and MaxCLL (content light level) features allow a display device to adapt the luminance, thus rendering both to its capacity and its recommended power-consumption limitations. The projector supplier has also planned to assess potential power-savings associated with HDR through laser dimming. In addition, this supplier is also investigating the impact of lower energy in the various WCG modes.

Growing interest and demand

Crucially, availability of native-UHD content is an important driver of this new technology, and important events are good generators of such material. A case in point was the 2016 Brazil Olympics where Olympic Broadcasting Services and Japan's NHK distributed UHD coverage to cable, satellite, telco providers and other partners. This will further help promote and spread the use of UHD.

In addition, over 14 product prototypes or technologies have been developed along the UHD value-chain. This confirms the huge impact of UltraHD-4U on project partners in their IPR building and dissemination, and their drive to be well prepared for the market ramp-up.

Furthermore, a crucial survey among some 500 video-service providers and content producers concluded that 96% of them believe that a majority of consumers and operators will adopt UHDTV by 2020; and 88% of total respondents said they will launch UHDTV content by 2020. Notably, 78% believe consumers are willing to pay 10-30% more for their subscription for access to UHDTV content.

Comparing the global UHD market forecast in 2013 with that in 2016, we see that meeting the key annual-shipment 'threshold' of 100m UHD TV sets was initially foreseen to happen in 2023. However, in 2016 it was expected to take place in 2019, with around 50% shipping to Asia-Pacific, 25% to Europe and 20% to North America. However, due to lack of available UHD content, not all these UHD TV sets will be showing a native-UHD stream, but mostly converting the HD stream into UHD, internally.

A study by Research & Markets, published in early 2018, says that there will be acceleration in the adoption of 4K technologies, with compound average growth rates (CAGR) of some 20% in value by 2022. This study also states that growth will come from a 'surge' in the adoption of 4K projectors and 4K cameras in the media and entertainment industry; increasing per capita income; and improvements in the standard of living.

Finally, according to a new report by Grand View Research published in June 2017, the global 4K TV market is expected to reach US$ 380.9 billion by 2025.This is excellent news for consumers and the global television industry alike.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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PROJECT RESULTS

CA206 | Advanced e-Passport makes border control faster, easier and more secure and also offers travel services [NewP@ss]

Deploying microelectronics and embedded software, the NewP@ss project delivered advanced secure platforms for third and fourth generation e-Passports, currently under discussion at the International Civil Aviation Organization (ICAO). Once approved, the new e-Passport could be deployed for European and international travel, and to host a variety of travel-related e-applications – from electronic visas and boarding passes, to airline services.

NewP@ss focuses on developing advanced and secure platforms capable of handling new generation e-Passports for European and international travel. The third generation e-Passports were expected to be put in place in Europe by the beginning of 2015, and fourth generation ones in 2018. These new platforms enhance security and features traditionally connected with a passport, and can host dedicated e-services associated with travel. In fact, several other related e-documents, including the residence permit, are currently being finalised. And other electronic applications including e-Identity, Register Traveler Program, electronic voting and electronic driving licence are under consideration

This project is also about addressing interoperability, as well as, contributing proactively to international standards.

High performance and tight security were top priority

The NewP@ss project targeted the development of advanced microelectronics and embedded software secure platforms for the future generations of e-Passports and related government and private-sector e-services. To achieve project objectives, NewP@ss also made use of results and deliverables from previous CATRENE projects, such as MEDEA+, Onom@Topic and BioP@ss.

Project activities were quite extensive and included developing:

- Hardware and software technologies to support next-generation e-Passports, and in particular, the new logical data structures (LDS2) under discussion at the International Civil Aviation Organization (ICAO). This will enable a fundamental conceptual shift on passport usage, and also make the e-Passport a true multi-application device;
- Technology elements to meet regulatory performance and functionality standards. These include new cryptographic protocols (like SAC, EAC v2.1); high-speed contactless interfaces (like VHDR/VHBR); and efficient biometry;
- Complete proofs-of-concept for new e-Passport implementation, resulting in a combination of advanced secure microcontrollers; advanced embedded software platforms based on small footprint multithread OS; and secure compact fixed or mobile readers. Validation was done through use cases deploying typical e-government and private organisation scenarios. Some of these use cases required development/validation of security mechanisms for the proper handling of security credentials (such as certificates and PKI schemes);
- Security and privacy concepts needed to ensure a lifespan of five to 10 years for e-Passport platforms, as well as, the proper level of isolation between applications;
- Functional test suites and reference implementations suitable for further interoperability testing.

Project results are very encouraging. Deliverables include advanced secure e-Passport platforms embedded with state-of-the-art, near-field communication capabilities, which are 16 times faster than the generation of passport currently used. Microcontrollers provide the necessary computing power and memory to achieve high computing performance as well. Associated readers with impressive performance and interoperability requirements are also available. And with the increase in fraudulent activity, there was a special focus on security and privacy aspects, resulting in the implementation of new, very effective cryptography protocols (like SAC and EACv2.1). Crucially, the NewP@ss platforms have reached the highest level of security required for border-control operations. The first 3G ePassports are now available and will be marketed in 2016; and the 4G version from 2018.

PROJECT CONTRIBUTES TO

- Communication
- Safety and security
- Digital lifestyle

PARTNERS

Gemalto
NXP Semiconductors F
id3 semiconductors
STMicroelectronics
Compuworx
Infineon Technologies
Giesecke & Devrient
NXP Semiconductors G
Infineon Technologies
NXP Semiconductors A
EVOLEO Technologies
Institute CEA-LETI
ISEN-Toulon
Instituto de Telecomunicações Aveiro
TU Graz Institute for Applied Information Processing and Communications

COUNTRIES INVOLVED

- France
- Germany
- Hungary
- Austria
- Portugal

PROJECT LEADER

Jean-Pierre Tual
Michael Guerassimo
Gemalto

KEY PROJECT DATES

July 1, 2012 - June 31, 2015

Promoting European expertise, standards and industry

Information sharing within the NewP@ss consortium was very effective: more than 50 reports with project results were shared internally and new collaborations have been established. Project partners also shared project knowledge and scientific results in academic journals, and through major international conferences. In addition, the consortium contributed to various special-interest groups focusing on standards and applications.

NewP@ss goals and deliverables mesh nicely with the European Union's own Digital Agenda that sets out the European Commission's strategy for addressing the main challenges and developments in the information society and media sectors up to 2020. This initiative aims at improving efficiency, modernising administration, reducing bureaucracy and facilitating citizens in communicating with the various administrative authorities. Once citizens have secure national identification cards and e-Passports, they will be able to gain easy access to services in an expanded e-administration.

In the travel world, the European e-Passport scheme is considered a showcase and reference. This means, for example, the new SAC protocol could be supported globally through this project, thus promoting European standards and industry in the process.

Business opportunities with e-government services

Identity management (the mechanism for identifying a person) is currently conducted mostly by paper. Electronic identity will complement, or perhaps even replace, paper-based identification with electronic means, which offers huge advantages, such as information access anytime, anywhere. A good example of where identity management can be deployed is in accessing public services, something every EU citizen is entitled to. Importantly, this should be simple, secure and accessible anywhere and anytime within any member state.

However, implementation raises several technological and organisational issues. These include security, privacy and data protection, together with interoperability and the amount of information an ID card should contain, as well as the means and methods of authentication. NewP@ss makes this possible by providing some of the key enabling technologies and components, together with the necessary expertise and experience. It in fact offers a sound basis for developing new business models around e-government services.

Markets to match

Applications targeted by the Newp@ss project share stringent requirements in terms of security and interoperability at European and international levels. That is why this project strengthens the competitiveness of the European industry for e-Passport and other spin-off applications and services that use secure personal devices. Furthermore, these applications have large economic, societal and technical impact and will represent a huge part of the total e-Passport market by 2015-2020. In fact, this market is vast and expanding. Already more than 30 countries adopted the first version of the ICAO e-Passport by mid-2007, and the EU adopted SAC-secured biometry at the end of 2014. Adoption in Europe of third and fourth generation e-Passports is expected to create a market for more than 200m units.

And notably, Secure ID News predicted in 2010 that the e-Passport market (made up of hardware, software, and services) would reach sustainable, annual revenues of US$7 billion by the end of 2014, with a compound annual growth rate of 31.5% in 2009-2014. In addition, the Asian market is expected to experience the most significant market-share growth, increasing from 25% to nearly 46% of annual market revenues with an annual compound annual growth rate of nearly 50%.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

PROJECT RESULTS

CA310

Resolving electromagnetic compatibility and reliability issues benefits electric vehicle and automotive and semiconductor industries alike [EM4EM]

This project handled important design challenges with electric and electronic components associated with building electrically operated vehicles. Typically, it deals with electromagnetic compatibility and electromagnetic reliability issues of communication units, which resulted in a significant reduction in electromagnetic emission generated by electric powertrain components.

Designing and developing electrically operated vehicles (EVs) bring with them huge design challenges with electric and electronic components. Electromagnetic compatibility and electromagnetic reliability of communication units, for example, will require a significant reduction in electromagnetic emission generated by the electric powertrain components. What is needed, in short, is for the automotive and semiconductor industries to provide solutions that offer noise immunity in nanoelectronic components and electronic modules.

Holistic approach to electromagnetic compatibility and reliability

Taking a closer look at the technical issues, we see that the close vicinity of high field strength from high-voltage cables and electric motors, and sensitive high-density electronics, requires a holistic approach to electromagnetic compatibility (EMC), respectively electromagnetic reliability (EMR). To complicate things further, the commonly used shielding effect of the car's metal case will disappear due to lightweight designs using carbon fibre cabinets, for example. Furthermore, the introduction of the electric powertrain establishes new voltage and power levels in the vehicles. Therefore, suitable EMC/EMR design and related measures, not previously dealt with in a structured manner, are required.

EM4EM tackled these problems by, firstly, introducing solutions that dealt with noise immunity issues with nanoelectronic components (such as ICs, sensors and power devices) and electronic modules needed in future developments in the automotive and semiconductor industries; and secondly, by introducing methodologies to reduce electromagnetic noise-emission generated by power electronic components, modules and systems, and to increase, on the other hand, the noise immunity of sensor systems. Notably, the project also improved time-to-market and cost efficiency.

Key project results were as follows:

- A new IGBT module design using a symmetric H & L bridge layout demonstrated a further reduction, on the semiconductor level, in noise levels of up to 15 dB at low frequencies (less than 10 MHz);
- A new bulk current injection (BCI) setup for measuring an extended frequency range between 100 kHz and 400 MHz was developed;
- On the component level, a new ringing active control method for PWM driver transistors (based on ringing measurement but without time-consuming calculations based on a fully adaptive algorithm) was developed and tested;
- Innovative new algorithms for tuner integrated EMI (electromagnetic interference) suppression for AM, FM and DAB broadcast services were developed and integrated on a system and vehicle level;
- Most recent measurements show that the SNR was improved by about 10-25 dB. Integration and demonstration activities with a European chip supplier are underway;
- A new measurement methodology to define initial EMR conditions for HEV/PHEV/EV was introduced. A mandatory part was the research on the material level to qualify suitable lightweight materials (like carbon fibre reinforced polymers) for weight reduction, and to ensure electromagnetic shielding behaviour. These are essential for addressing environmental challenges of CO2 emission.

For validation and further exploitation purposes, a set of 26 demonstrators on all four application tiers – semiconductor, component, system and vehicle – were developed to be used in initial products based on EM4EM-developed technology. This included a complete demonstrator based on a test EV called the eBuggy. It consists of real EV components and cables, and offers easy access to all relevant parts of the vehicle. Furthermore, the eBuggy will continue to be available to EV developers to do further investigation and analysis work in a realistic EV environment.

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Energy efficiency
- Design technology
- Process development
- Manufacturing science

PARTNERS

AUDI AG
Daimler AG
Infineon Technologies AG
Conti-Temic microelectronic GmbH
Robert Bosch GmbH
NXP-Semiconductors Germany GmbH
ZUKEN GmbH
ELMOS Semiconductor AG
Leibniz Universität Hannover
Friedrich Alexander Universitaet Erlangen-Nürnberg
Technische Universität Dortmund
CTU – Czech Technical University Institut of Microelectronic Applications Ltd.
VTT Technical Research Centre of Finland
Okmetic Oyj
Murata Electronics Oy

COUNTRIES INVOLVED

- Germany
- Czech Rebublic
- Finland

PROJECT LEADER

Jörn Leopold
AUDI AG

KEY PROJECT DATES

March 1, 2013 - March 31, 2015

Centre of expertise and influence

In handling important areas of nanoelectronics development and EMR research, and new methods to improve electrical vehicles and industrial electronic systems, EM4EM not only resolves key technical problems affecting EVs; it will also have some potentially beneficial (commercial) spin-offs. For example, its target to reduce the overall EMR development effort will increase the competitiveness of the European automotive and semiconductor industry on the world market, as will reliable operating-equipment integration, optimisation, safety and robustness, main project objectives. Importantly, the project consortium will also influence other key EV development and production activities and processes, and its drive towards European co-operation will accelerate acceptance and implementation.

Healthy markets

Now, EVs require a huge variety of new electronic functions in propulsion, diagnostics, driver-support, navigation and vehicle-to-grid communications. Taking advantage of these innovative market opportunities requires the special expertise and experience found in semiconductor manufacturers participating in EM4EM. And the trove of project deliverables – including tried-and-tested models, measurement methods and procedures, together with simulation tools and methods – can be used by other European businesses to reduce the time-to-market and costs of EMR-optimised components and systems for EVs. And demonstrators will help third parties integrate these results quickly into new products, helping European industry deal with EV components and systems, and related products.

Project deliverables will also secure and expand European companies in the automotive industry, as well as, preserve – or even increase – employment in Europe and ensure a stable R&D. The market for EV-related products and services – including those deploying EM4EM competence and deliverables – will grow. By 2020, there will be a market for more than 13m electric vehicles requiring multiples of electronic components (compared to today's combustion-engine vehicles), and providing a huge potential for system and semiconductor manufacturer or supplier. Power semiconductors and modules, in particular, will experience a tremendous economic boost in the upcoming years. The semiconductor market for hybrid- and battery-electric vehicles with annual growth rates of 25%, is expected to increase to US$5.5 billion in 2020, reaching about 15% of the overall automotive and semiconductor markets.

And the added-value from electronics in cars will continue to grow steadily, with the share in the value of cars rising to 32% by 2015, thanks to the electrification of the powertrain and cost- and energy-efficient car technologies. In addition, time-to-market will get shorter as productivity from these new technologies kicks in much faster. And, at an annual growth of around 10%, the total automotive-electronics market will stay very attractive in the future.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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PROJECT RESULTS

CA701 | A novel unified design methodology for the virtual prototyping of heterogeneous systems [H-INCEPTION]

H-Inception delivered a unified design methodology and tools to address the virtual prototyping of heterogeneous systems. This was largely in response to the problem with errors that often occur and are recognised too late in the design cycle, thus causing additional design spins and delays. This project ensures that industry performs system-design verification very early in the product development cycle, decreasing the time-to-market and system costs.

Consider the following (business) scenario. New types of emerging applications require microelectronics with embedded software which closely interacts with the surrounding environment in different physical domains – like optical, mechanical, acoustical and biological. However, design errors, such as functional incorrectness, wrong interfaces, or non-compliance (with the initial product specifications) often occur and are recognised too late in the design process. This leads to additional design spins and delayed schedules due to necessary reimplementation, which in turn disrupt marketing plans and launch targets. What to do?

Focusing on three key components

H-INCEPTION's response is a novel, unified design-methodology, and requisite tools to provide system-level design and verification for new types of emerging applications, especially those which require microelectronics to closely interact with the surrounding environment in different physical domains. It also proposed providing European industry with an ecosystem that delivered all the design-technology ingredients: from design and verification methodology to the essential modelling languages, together with simulation engines.

In order to address the virtual prototyping of multi-physical systems controlled by embedded software, H-INCEPTION proposed three key innovations:

- A methodology for system design, architecture exploration and verification;
- A 'correct by construction' approach for the integration of multi-domain systems;
- A system simulation framework.

Key project activities that followed are grouped as follows:

- Specifying multi-physics extensions (to IEEE standards) for P-XACT and SystemC;
- Development of the proof-of-concept simulator that embeds computational models for physical domains;
- Development of a framework;
- Validation of the key innovations through industrial applications.

H-Inception developed and delivered a framework with a simulator that validated the project results and deliverables through seven use-cases, covering wireless, consumer electronics, automotive, medical and printing. Key to the success of the project was the re-use and extension of two standard computer languages – SystemC for simulation and IP-XACT for model management and flow automation – widely deployed in industry for digital systems with embedded software, and whose capabilities the CATRENE project Beyond Dreams extended to analogue and hybrid systems.

Promising technical and operational benefits

A single kernel simulator based on SystemC extensions avoids the use of multiple simulators and their associated license costs. Furthermore, thanks to IP-XACT, the database is not proprietary and can be easily shared. The simulator is now available and can be downloaded freely from the H-Inception website. Industrial partners are deploying the methodology in the development of new products. Encouragingly, partners are integrating project outcomes into their tool offerings and services; and academic partners are promoting the languages in their courses. Project results are also expected to be reused in new collaborative projects.

Another project deliverable, the complete and open framework, is already available. It offers end-users a graphical interface with schematic entry, design assembly, checking and net-listing, together with useful links to the simulator. This framework is crucial to multi-physics system-developers who are used to working with such an interface. Furthermore,

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Health and aging society
- Design technology
- Sensors and actuators
- More than Moore
- More Moore

PARTNERS

STMicroelectronics
Continental Automotive France SAS
Magillem Design Services
COVENTOR
ATRENTA
Brio Apps AlphaSip
Université Pierre et Marie Curie
Ecole Centrale de Lyon
Ecole Polytechnique Fédérale de Lausanne
Holst Centre / IMEC-NL
Océ Technologies
Dizain-Sync
Reden Holst Centre/ Imec-NL
SmartSigns
TU Delft (TUD)
Associate partners & Contractors
Fraunhofer IIS/EAS
Universidad de Cantabria
Universidad de Zaragoza

COUNTRIES INVOLVED

France
Spain
Germany
Netherlands
Switzerland

PROJECT LEADER

Olivier Guillaume
STMicroelectronics

KEY PROJECT DATES

December 2012 - December 2015

a common database for software, digital and multi-physics facilitates the communication between experts in a particular field.

Importantly, the virtual prototyping of seven applications for validation purposes also delivered and quantified such benefits as cost reduction, time savings and performance improvements – key criteria for time-to-market improvements. Test results were also most promising. Cost-reduction stood at 60% for the prototyping phase, and 15%-30% for manpower. Development time of the prototype was reduced by about 50%, from three to six months, thanks to the early development of software ahead of availability of hardware, and also to the re-use capability of the models.

On the performance side, virtual prototyping allows the simulation of multiple effects and hence increases design knowledge leading to system optimisation in such application areas as injection system for automotive applications; the autofocus speed in optics; MEMS control; and the optimised quantity of fluids in biomarkers.

Reinforcing Europe's leadership positions

There are also other types of benefits. To start off with, enabling technologies provided by H-INCEPTION will significantly improve the competitive position of European industry by allowing the co-designing of microelectronic platforms, and enabling European semiconductor companies and OEMs to keep pace (and outperform the competition) in the face of increasing complexity and heterogeneity required to maintain their leading position in system design and integration. SystemC, with its open-source, proof-of-concept implementation, will ensure European industry keeps its leadership position in the application of advanced system-level design methodologies and tools. This will also result in better, high-quality products and systems, which will be available earlier on the market.

Furthermore, European semiconductor companies producing 'correct by construction' prototypes and delivering these virtual solutions to their system integrators will be able to reduce development time by six to ten months. Industrial partners will therefore be in a leading position to match customer demand and save development costs by introducing new 'proof-points' and reducing design iterations in the total value chain. This know-how will further strengthen Europe's pole-position in MDVP products and solutions, resulting in increased European competitiveness and employment.

Environmental, safety, security and healthcare improvements

And there are plenty of other areas where H-INCEPTION's effects will be felt. Project simulation demonstrates how optimising a vehicle's injector system can reduce vehicle CO2 emissions; and how costs and development time at a biomarker lab are significantly reduced, thus facilitating cardiac-disease detection. In addition, devices and embedded systems will offer more functionalities based on (wireless) connectivity and communication with their environment. Typical applications include toll payment with mobile phones; enhanced car-safety through road/traffic monitoring; using e-Passport for secure (internet) payments; wireless sensor networks for healthcare monitoring; and sensing technologies to improve, for example, the safety and comfort at work. Notably, these will go a long way to help support and secure European competitive power.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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PROJECT RESULTS

CT210 | New FDSOI design platforms can handle complexities of next-generation mobile devices [DYNAMIC ULP]

Technical advancements in mobile communications are in turn making mobile devices a lot more complex in design. In response to these demands, the DYNAMIC-ULP project developed two new design platforms for European manufactures. These are based on CMOS, commonly used in today's computer microchips, and FDSOI, a new competitive technology simplifying the manufacturing process.

By 2025, some 50 billion everyday appliances could be communicating wirelessly with other devices through the internet of things (IoT). Combine this with the mobile society's appetite for increasing amounts of multimedia content and additional functionality, and the result is a demand for even faster mobile networks based on LTE-advanced – the enhanced long-term evolution (LTE) mobile-communications standard – with transfer rates of more than 100 Mbit/s, and access to multimedia contents with no latency to the user. Crucially, this is making next-generation devices more complex, and a rapid increase in gate density will not address this complexity on its own.

Delivering two key FDSOI-based design platforms

What is really needed is an efficient design platform that will handle product requirements covering a wide dynamic range, from 1.1v (to enable processors to run at 3.25 GHz) down to 0.4v (for long multimedia playback). Among the key chip technologies deployed today FDSOI (fully depleted silicon on insulator) is the most advanced planar technology, and is able to significantly boost the performance or save a huge amount of power. DYNAMIC-ULP developed advanced process modules and contributed to two successive generations of FDSOI design platforms based on the 28nm and 14nm technologies for European manufacturers.

The project produced several key results and deliverables. At process and device levels, 14nm FDSOI technology was developed leveraging on the so-called body bias effects for a full FBB approach (high body bias). Looking to the future, studies and measurements conducted on SSGOI (strained Si/SiGe on insulator) showed that this process can ensure the scalability of the planar FDSOI device architecture for the 10nm node.

It fully confirmed SSGOI device-performance benefits. Compared to the 28nm FDSOI technology, the 14nm FDSOI device developed provides 0.55x area scaling, and delivers a 30% speed boost at the same power, or a 55% power reduction at the same speed. In addition, dual patterning was also introduced in the 14nm. The number of metal layers at 14nm node in UTBB FDSOI will be 11ML.

Furthermore, Dynamic-ULP provided the first FDSOI design platforms in 28nm and 14nm, including FDSOI design kits with spice models. A comprehensive test-chip strategy valid for both the 28nm and 14nm was used during the project in order to assess the performance of the technology and qualify the design platform. All IPs (intellectual properties) in 28nm FDSOI were validated, and the 28nm FDSOI has been qualified for volume production (Maturity 30) since end-2013.

FDSOI-based methodologies included methods for SRAM (static random-access semiconductor memory) development and design of specific logic (intellectual property firmware) blocks: variability analysis of SRAM bit-cells and SRAM 32kb circuits; feasibility studies to integrate forward and back biasing and DVFS (dynamic voltage and frequency scaling, a power-management technique); and development of a new test chip to connect the relevant IP blocks into a front-end receiver chain designed for LTE application.

New or improved commercial tools are ready for deployment. A new CAD (computer-aided design) tool for SRAM and standard cell verification (based on Monte-Carlo simulation) was developed, which shows an 8x speed improvement on standard tools for the industry. The efficiency of high performance/low power solutions was proven in most conditions and adapted in the case of low energy gains. Several techniques were developed that reduce the memory power of the design automatically. New cells were proposed for high energy efficiency and variability management also progressed, thanks to new mathematical methodologies. Furthermore, this project demonstrated improvements in 23 metrics.

PROJECT CONTRIBUTES TO

- Communication
- Energy efficiency
- Digital lifestyle
- Design technology
- Process development
- More than Moore

PARTNERS

ST-Ericsson STMicroelectronics SOITEC
CEA-LETI ACREO
Infiniscale DOLPHIN
Atrenta-France
Ericsson Mikroelektronik Ar-Ge Merkezi A.S.

COUNTRIES INVOLVED

- France
- Sweden
- Turkey

PROJECT LEADER

Philippe Garcin
STMicroelectronics

KEY PROJECT DATES

January 1, 2012 - December 31, 2014

DYNAMIC-ULP was a close collaboration of five partners from France, Sweden and Turkey. The project's R&D activities included 36 conferences and publications, invitations to give four lectures, and four Master's and PhD theses on subjects relevant to this project.

Stimulating the whole value chain

There are also commercial gains. After 15 years of constant growth, the mobile wireless market is now mainly fuelled by the replacement of outdated devices with smartphones and tablets, and also the emergence of new devices such as the "wearables". This has created a new segment with double-digit growth, and this project supports the European effort to gain a leading position in electronic industry by enabling design and production of FDSOI CMOS technologies in Europe.

The strategic nature of the semiconductor industry has been recognised around the world, and this recognition has led to the continuous emergence of new geographic regions as future semiconductors hubs, acting as a powerful engine for economic growth and high quality jobs. In addition, the research intensity in semiconductor is proportionally higher than in any other industry and provides an adequate incentive to reinforce the presence of upstream industries, such as semiconductor equipment manufacturers and material providers. The association of R&D activities with volume production and strong manufacturing facilities also has a profound impact in developing local ecosystems.

Vital for manufacturing

The IC industry has been one of the fastest growing industries over the past 30 years, primarily because it has been able to offer a continuously decreasing cost per function to the electronics industry. This rise in economic value is the main reason, explaining the success and proliferation of integrated circuits in our daily lives. For manufacturing, improving and developing tools and methods to effectively manage this highly complex mix of technologies, processes and products – something DYNAMIC-ULP is contributing to achieve – is playing a critical role in ensuring the future viability of the manufacturing facilities of our industry in Europe.

Europe cannot keep innovating without a powerful manufacturing base. This makes it necessary to maintain advanced prototyping activities in Europe, since it is the basis of future production runs and it may well help relocate production activities into Europe. DYNAMIC-ULP's design platforms in FDSOI 28nm and 14nm technologies will help achieve this, by joining with system architects, chip designers, CAD vendors and manufacturers.

Looks promising

Among the metrics where this project scored high marks, twelve of them concerned power reduction, indicating the importance it placed on ultra-low power techniques. Not surprisingly, it offers attractive solutions for the mobile industry, but also for the consumer market, IoT, green applications and more. Notably, good results recently obtained by Sony from an ST 28nm FDSOI test-chip implementation of a global navigation satellite system show that the penetration of FDSOI technology associated with efficient design methods is underway.

Finally, there are clear benefits from having the ability to remain competitive and at the leading edge of technology for job creation and retention in the European Union. The project involves multiple European countries and enables further employment opportunities in the future due to the new innovations being advanced in the project, especially enabling advanced manufacturing to continue, and a more fertile market for SOI wafers.

CATRENE Office
9 Avenue René Coty
F-75014 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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PROJECT RESULTS

CT213 | Biosensor platform impacts cost, accuracy and speed of drug detection, heart monitoring and diagnosis in healthcare [3DFF]

With the cost of diagnosis rising in countries with ageing populations, healthcare institutions are understandably seeking ways of deploying new technologies to produce low-cost, fast and accurate diagnostics and analytical systems to keep costs in check. That is why the biosensor platforms – 3DFF project deliverables based on a flexible substrate, and where biosensors combine high performance with low cost – are such a fitting response to these requirements.

Microfluidics is a technology in which tiny amounts of liquids can be used to lower the quantity of reagents and other materials, thus reducing the volume of body fluids used in analytical applications, together with many other benefits. Combined with different types of sensors, this technology can be used to produce small, user-friendly and affordable monitoring and detection devices. However, most of the materials used in marketed products are rigid and the integration of electronics in the chips is often difficult. Developing a broad spectrum of mechanical properties based on a flexible substrate and enabling electronic integration, could lead to interesting security and healthcare applications to assist an ageing population.

Fast, accurate and cost-effective devices for and multiple applications

In a nutshell, the 3DFF project developed a flexible sensor technology to provide accurate, fast, affordable and cost-effective biosensors with a broad range of applications: from security, in vitro medical diagnostics, to in vivo medical diagnostics. This technology is based on a flexible substrate that can integrate seamlessly microfluidic and microelectronics components. It will also form the basis of a disposable sensor which will be complemented with a reader platform able to translate sensor data into information which can subsequently be then presented to the users.

The 3DFF project activities included:

- Market research for defining market opportunities and user requirements;
- Developing microfluidic chips in different materials and with different properties (flexible, semi-flexible and rigid) designed for active and passive fluidic handling;
- Developing biocompatible flexible interphases for skin adherence in wearable devices;
- Developing novel electrochemical biosensors and a piezo-electric sensor;.
- Integrating sensors in flexible structures;
- Developing electro-chemicals;
- Developing three platforms corresponding to use-cases;
- Validating the platforms through animal models or by using biological samples.

Key project deliverables were three application platforms:

1. Drug-of-abuse (DOA) detector: A quantitative rapid illicit-drug-detection device for roadside police controls which is the first of its kind (there are only qualitative detectors currently). It includes microfluidic disposable cartridges (for avoiding cross- contamination) and an electronic reader;

2. Cardiac body-patch: A flexible patch with a novel piezo-sensor which led to a miniaturised cost-effective patch for cardiac monitoring. The device is capable of wireless communication with a PC for data acquisition in real-time;

3. Flexible skin-patch with chemical sensor: A microfluidic chip containing a qualitative rapid test stripe for detecting alarming-levels of morphine in sweat, for palliative-care patients.

Supporting European industries and development

Co-operation among project partners with just the right attitude was key to successfully dealing with technical problems and management issues. In general, the project benefited from good interactivity between small and large companies. A good example is the piezo-sensor, where good synergy between two project partners made its microfabrication possible. Technology transfer also helped the project, especially public research centres and small- and medium-sized enterprises (SMEs), where a good balance between new, advanced technologies, and market pragmatism was attained..

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Health and aging society
- Safety and security
- Digital lifestyle
- Design technology
- Sensors and actuators
- More than Moore
- More Moore

PARTNERS

Toppan Photomasks (TPI)
Alphasip (ASIP)
BodyCAP
Hemosoft
Boschman (BT)
Advanced Packaging Center (APC)
Laboratoire de Photonique et de Nanostructures – (LPN)

COUNTRIES INVOLVED

- Spain
- France
- Turkey
- The Netherlands

PROJECT LEADER

David Olea Duplan
Alphasip

www. 3dff.eu

KEY PROJECT DATES

December 10, 2012 - November 30, 2016

There are also spinoffs that could benefit the semiconductor, healthcare and allied industries in Europe (and beyond). By mixing polymers with micro-electronics, the project reinforces the research policy of the European Union (EU) concerning electronics fabrication in Europe. This creates new applications, instead of just competing for the smaller chip technology. Biomedicine and other sectors can also benefit from these new developments.

3DFF also supports the development of a European system-in-package (SIP) supply-chain for innovative systems and differentiating technologies through 3D (three dimension) and heterogeneous integration. The development of a 3D integrated microfluidic technology – a 3DFF objective – will ensure features, like multiplexing, flexible reception systems, miniaturisation and heterogeneous integration, are included in the development of SIPs, thus ensuring different application areas also benefit.

Likewise, innovative technology addressed in 3DFF, could clearly promote European leadership in the supply chain for 3D/SIP by exploiting existing strong interaction between technology development and application domains. For example, this project applies developed technology in two application domains: roadside drug-screening; and healthcare in vitro diagnostics, where a point-of-care (POC) device is used to help rule out, among other conditions, deep vein thrombosis (DVT).

And by ensuring competiveness in three European healthcare sub-sectors – security, in vitro diagnostics and health monitoring – 3DFF seamlessly ramps up the concept from prototype (feasibility) through various designs in a single, flow-to-mass fabrication. It also creates a large application field to produce chips with the reliability, speed, pitch and pin count necessary for optimal performance, including lower-power usage, and a faster time-to-market.

Vibrant markets

The expected impact of this project is significant because of the high market-volume on which 3DFF is focused. Firstly, an accurate and cost-effective POC test for cardiovascular disease (CVD), for instance, will increase survival after a thromboembolism (a combination of thrombosis and embolism) and also effectively reduce costs. POC use of CVD is gaining in popularity, with an estimated market of US$ 830m in 2008. This means targeting EU (27%) and North-American (45%) markets – where an unhealthy stressful and sedentary way of life is prevalent – makes good commercial sense.

Then there is drug-testing. With European authorities strongly promoting road safety through strict policies against driving under the influence of drugs, such a reliable, low-cost, portable drug-screening device would be ideally placed to significantly decrease the number of road accidents. There are also broader potential markets for this product. Global estimates suggest that the economic costs of road traffic injuries amount to US$518 billion annually. In developing countries, the costs are estimated at US$100 billion, twice the annual amount of development aid to developing countries.

And that is not all. 3DFF introduces a synergy that could lead to the creation of new R&D projects involving consortium participants. Furthermore, knowledge acquired in this project will drive technological transfer applicable in other areas. 3DFF will also promote the different R&D areas of this project and foster new research lines. This could directly affect job creation linked to production and sales of demonstrators developed in 3DFF. In the long term, this technology could even increase European employment, creating more than 200 jobs for manufacturing these devices, and 100 jobs in research, administration, finance and sales.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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PROJECT RESULTS

CT312 | Transforming quality in R&D of 3D integrated circuits into leadership in sustainable 3D IC manufacturing [MASTER_3D]

The project MASTER_3D aimed at reaching excellence in three dimensional, integrated circuit production by developing and implementing methods that raise the quality of manufacturing and also make it cost-competitive. This project focuses on process and equipment innovations, metrology, testing and yield, with a special emphasis on through silicon vias (TSV) and wafer level packaging (WLP).

3D integration is considered a key technology for heterogeneous system integration, and the ongoing merge of semiconductor front-end and assembly and packaging technologies is now part of scaling and functionality roadmaps for 2.5D/3D solutions. In the process, Europe has gained R&D leadership in this field. Before MASTER_3D was conceived, however, there was a risk that Europe would fall behind its Far-Eastern competitors if it did not raise quality levels of its manufacturing as well. This meant creating the right 'production environment' to allow it to play a significant role in the volume manufacture of 3D integrated circuits (ICs), precisely the objective of MASTER_3D. In the process, this project is turning European Union leadership in the R&D of 3D integrated circuits, into one in sustainable 3D integrated IC manufacturing.

Targeting manufacturing excellence

MASTER_3D aimed at quality in 3D IC production through cost-competitive manufacturing methods that deploy through silicon vias (TSV) and wafer level packaging (WLP), as well as in-line and electrical parametric monitoring, with yield enhancement and testing,

Key project activities and deliverables can be summarised as follows:

- Process tools assessment and improvement for mass production: related to the enhancement of the unit process robustness in the context of process specifications and process stability, as well as cost-of-ownership of process equipment;
- Characterisation and metrology: the development and assessment of necessary methods and tools to characterise and control 3D-specific process steps;
- Validating test infrastructure: testing out a product-compatible test infrastructure and its integration into a 3D industrial test-flow;
- Yield modelling and testing: demonstrated the technology and assessed project progress and results.

Information sharing was excellent. The project generated some 45 reports and 50 presentations, and project results and knowledge shared internally, as well as, with academia and industry. Innovation and creativity were not in short supply, with the submission of six patent applications, and two project partners created a common laboratory. Project partners also addressed the issue of standards for memory interfaces, computer aided design (CAD) tool formats, and test interfaces, with many partners initiating their own standardisation initiatives.

Spin-off benefits for project partners

The composition of the consortium meant that partners contributed the right expertise and skill-sets necessary for 3D manufacturing, and ultimately to the success of the project. Excellent collaboration that was established and emphasised in the course of this project also contributed to technical results considered beyond state-of-the-art.

MASTER_3D partners are now well positioned to take advantage of market opportunities.

3D stacked dynamic random-access memory (DRAM) and advanced logic interposers are now in production and most of the tool suppliers involved in the project have already sold tools for these applications. This first TSV adoption phase also provides a good opportunity for all participants to accelerate tool and process improvements and therefore facilitate TSV-based products to become profitable.

However, the main driver of MASTER_3D is coming from heterogeneous integration. More and more opportunities are emerging in the field of silicon photonics (an evolving technology in which data is transferred among computer chips by optical

PROJECT CONTRIBUTES TO

- Automotive and transport
- Energy efficiency
- Sensors and actuators
- Process development
- Manufacturing science
- More than Moore

PARTNERS

ALES
ams AG
AXO
CEA-LETI
CNRS LIRMM
EVG
FhG (IWMH, IKTS-MD, IZM)
Fogale
IMS Bordeaux
Infineon
Sentronics Metrology
NXP
PVA TePla
QUALTERA SAS
Rockwood Wafer Reclaim SAS
SPTS Technologies SAS
STMicroelectronics

COUNTRIES INVOLVED

- Austria
- France
- Germany

PROJECT LEADER

Brigitte Descouts
STMicroelectronics

KEY PROJECT DATES

December 2012 - June 2016

rays) internet of things (IoT) and radio frequency (RF), for example. And project partners and other European companies are well positioned to address this huge system-in-package potential market.

Some 3D-specific techniques (such as polymer permanent bonding and stress compensation) are also valuable enablers for new applications. Some projects relying on these techniques (not necessarily real 3D Integration) have already been launched and are now considered key opportunities for innovation.

Broader markets, promising opportunities

There are also wider possibilities. Crucially, not only does MASTER_3D address user requirements and demands, but it can also benefit from markets needed to commercialise and monetise its deliverables. For example, with the implementation of 3D TSV in high-volume production, this memory technology is expected to reach US$4.8 billion in revenues by 2019.In addition to a strong demand for micro-electro-mechanical systems (MEMS), power devices will also continue to play a key role in the electrification of transport and changes to the grid infrastructure. (These two fields are being influenced by the combination of renewable-energy production and storage stations, and by political push towards cleaner transport systems.)

Then there is the lighting industry, which is now investing in LED modules to improve the quality of luminaires, reduce costs and improve value. With more industrial ventures initiating this transition in 2016, 3D CMOS image sensors (CIS) will represent 69% of the total wafer starts in 2019, followed by 3D stacked DRAM reaching 11% and wide I/O with 9%. Regarding revenue, CIS will represent 65% of the total revenue in 2019, followed by 3D stacked DRAM with 17% and 3D logic/memory with 9%.and wide I/O will represent 7% in 2019, but is expected to grow in the future.

Furthermore, advanced packaging is now part of the scaling and functionality roadmaps and providing additional interest in 2.5D/3D solutions. In order to respond to market demands, the advanced packaging segment is focusing on integration and WLP. Emerging packages, such as fan-out WLP, 2.5D/3D IC and related system-in-package solutions, aim at bridging the gap and reviving the cost/performance curve.

Notably, IoT and Si photonics provide additional opportunities. After all, more than half of all major new business processes and systems are expected to incorporate some element of IoT by 2020. Enhanced demand for high data-speed and communications by data centre applications have already resulted in significant growth in the global photonic IC market, which is expected to expand to US$497m by 2020, growing at a CAGR of 27.74% from 2014 to 2020. And the silicon photonics device market is expected to grow from around US$25m in 2013 to more than US$700m in 2024, at a 38% CAGR. Furthermore, emerging optical data centres owned by large internet companies (Google, Facebook and the like) could trigger this market growth in 2018, with Intel, which is very active in this field, contributing to a quick ramp-up of silicon photonics.

MASTER_3D reminds us that a project's success is not only measured by the quality and availability of its deliverables, and how well they mesh with user and industry demands; but also by market opportunities capable of turning them into revenue.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

CALL 5

PROJECT RESULTS

CA112

Customisable heterogeneous high-performance design platform facilitates high-throughput fault-tolerant applications [HARP]

In developing a customisable, heterogeneous design-platform, HARP's unified hardware and software architecture does not only improve design productivity. Crucially, its data-flow programming models and reconfigurable memory hierarchy also ease and quicken the design of future high-throughput, fault-tolerant systems running performance-demanding, high-reliability applications, ranging from aeronautics to video.

High-performance computing (HPC) has evolved remarkably over the past 20 years. However, mobility trends are pushing the computational boundaries even further with demands to process video, speech, healthcare, vehicle and environmental data faster and more reliably. Indeed, mobility is not only highlighting the need for electronic equipment to be very reliable, but to also reduce inherent risks. This, in turn, calls for high-performance design platforms to develop and run high-throughput, fault-tolerant applications, in an ever-reduced power envelope.

HARP increases performance and design productivity

Addressing these important issues, HARP developed a heterogeneous architecture which can be optimised for a given customisation level. It does this by integrating, in the same system-on-chip (SoC), one or several clusters composed of a mix of general-purpose and specialised processors, together with hardware intellectual property blocks (IPs).These IPs were developed by semi-automatic design-flow using high-level synthesis tools, and a data-flow programming model based on data-flow graphic descriptions. In this way, HARP achieved the best of both worlds: software offering flexibility and easy post-production customisation; and hardware providing high performance and a smaller footprint (hence lower costs).

HARP produced a set of new design techniques based on standards (like OpenMP), which it then applied to demonstrators, validating such application areas as aeronautics, computer vision and multi-standard video codecs.

The project also analysed the issues of multi-processing, both by quantifying and circumventing them. For example, performance-loss due to shared program cache memory was minimised. The metrics obtained on demonstrators confirmed the soundness of the HARP approach. At the design level, for instance, parallelisation showed a time-reduction from months to weeks; and simulation was faster by a factor of 600. And at the application level, throughput went up by a factor of 40; energy efficiency by a factor of 58; and silicon area was reduced by 20-30%.

Allowing Europe to stay ahead of the competition

In general, HARP will contribute to Europe's potential to compete in worldwide markets and, thus drive employment. This means it will not only safeguard high-qualification jobs in the European microelectronics industry, but also generate new jobs at small and medium-size enterprises (SMEs) and create opportunities by sharing high-tech results. Design productivity will also benefit from HARP's unified hardware/software design flow, dataflow programming models and reconfigurable memory hierarchy, thus facilitating the design of high-throughput, fault-tolerant applications. This enables high-performance products to be designed faster, and at a favourable price and with lower energy consumption.

But there are more benefits in store. HARP's deliverables will allow European industry to extend its portfolio of innovations with, for example, new encoding algorithms which could be used in many-core SoC implementations, thus allowing Europe to secure its reputation in MPEG video technology. In addition, performance-estimation techniques for mapping video applications onto heterogeneous platforms, and hardware IPs that increase the average performance of video applications will help broaden Europe's knowledgebase and product portfolio. And another 'soft' deliverable – its hardware/software co-design methodology – could be extended to deal with the movement of massive amounts of video-related data across the computing fabric.

Aeronautics is another key HARP target, where the high-level of hardware redundancy, a key safety requirement, represents up to two-thirds of the electronics' cost in a commercial aircraft. Thanks

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Safety and security
- Energy efficiency
- Design technology

PARTNERS

STMicroelectronics

AIRBUS GROUP

SAPEC

CEA

Universitat Autònoma de Barcelona

University of Cantabria

COUNTRIES INVOLVED

France

Spain

PROJECT LEADER

Philippe Garcin
STMicroelectronics

KEY PROJECT DATES

January 2013 - June 2016

to HARP's fault-tolerant computer architecture based on advanced arrays of multiprocessors, costs will come down and European suppliers of aeronautic systems will have a competitive edge.

Imaging is yet another area to benefit from deploying HARP-developed technologies. Smart cameras, deployed in the internet of things (IoT), will use less energy, and reduce bandwidth requirements and minimise privacy risk by doing image analysis on-chip.

Consumers will also be winners. Video-related products will be lower in price and come with increased video quality (compared to the current H264-AVC standard). There are also plans to double the ratio of data compression (with a resolution of up to 7680 x 4320 pixels).

Finally, conserving energy. Computing power is strongly correlated to energy consumption, and mobile equipment has limited access to permanent power sources. Energy efficiency is therefore a main part of HARP's requirements, and elements, such as low-power multi-core processors, will be key enablers in sustainable and energy-efficient projects.

Promising markets for imaging, video and fault tolerance

The business in which HARP will play a role looks promising. With device-to-device communications (where HARP's deliverables could be deployed) becoming widespread, Gartner forecasts 20 billion devices connected by the end of 2020.

Thanks to HARP, companies could also increase their share of the video market and help European electronics firms maintain their leadership position in set-top boxes (STBs). It does this by ensuring they are among the first (and ahead of the competition) to provide multi-standard video-codecs within the new, high-performance, highly efficient SoC generation, offering UHD5 (a version of ultra-high definition television) support and a short time-to-market. Furthermore, future video applications will create new business. The worldwide revenue for STBs is expected to exceed US$ 4 billion annually from 2016 on. With an 8% market share, a leading European electronics concern and project partner predicts revenue of US$ 1 billion and a 5% growth per year in STB unit shipments. And thanks to HARP-developed technology, revenue, gross margins and market share will also grow.

Then there is the worldwide market for HDTV H264 video encoders, which stands at around US$180m, with an expected CAGR (compound annual growth rate) of 6-7% in the next five years. New algorithms that reduce the bandwidth, and new TV systems like UHDTV and 3DTV, will drive this CAGR growth. And the 65% market share for Intel-based, video-analysis systems is projected to decline and huge gains are expected in the digital signal processing (DSP) market in 2014-2016. In addition, the market for computer-vision technologies will grow from US$5.7 billion in 2014 to US$33.3 billion by 2019, representing a CAGR of 42%.

And finally, aeronautics. The world's passenger aircraft fleet (above 100 seats) will grow from 18,500 aircrafts to 37,500 by 2033. At the same time, some 10,500 aircraft from existing fleets will be replaced by more eco-efficient models. Importantly, HARP's fault-tolerant system could be marketed by aircraft suppliers as a unique selling point, based on its benefits.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

PROJECT RESULTS

CA505

Towards the better management of power production, consumption and dissipation in smart mobile devices [BENEFIC]

Energy inefficiency and poor power management are obstacles in the way of smart mobile-devices: their potential growth and success in many sectors of society. Responding to this problem, the BENEFIC (or Best ENergy EFficiency solutions for heterogeneous multicore Communicating systems) project deploys a holistic approach in developing new ways to improve energy efficiency.

A new category of smart mobile-devices is invading our daily lives. They are always connected, and contain multicores which work at higher frequencies and under low, tightly controlled power-consumption constraints. Simple analysis shows that a maximum sustainable power-dissipation of 4W for a smartphone, and close to 15W for display devices which are larger than seven inches in size. A lot has already been done to improve power efficiency, but much more is needed to address these and other important energy-related challenges.

The total approach to power management

Important breakthroughs can only be achieved if the total energy chain in a system is addressed. Therefore, the main objective of the BENEFIC project is to provide a holistic approach to integrating new sources of energy-harvesting (the process by which energy is derived from external sources, like solar, thermal and kinetic) and innovative approaches of distributing energy closer to places where it is deployed. These new methods will allow for better prediction and management strategies for power consumption through the insight combination of elementary techniques from lower physical layers to middleware optimization targeting to improve the Performance/Power ratio by a factor 5 at application level.

The BENEFIC project is organised around five applications domains, for which ten physical hardware demonstrators were built to test and validate energy-related improvements that were developed. The following describes developments in each of the five domains:

1. **Professional communication**

- Improved low-power ARC processor: subsystem for low-power application for software-defined radio (SDR) in which measurements and power estimations are based on realistic applications, and not just synthetic benchmarks. This demonstrator succeeded to improve the Performance/Power ratio by a factor x6.25;
- Energy Neutral Operation (ENO) platform: main objective is to reach ENO for the wake up system supplied by harvesting. This demonstrator succeeded to improve the Performance/Power ratio by a factor x4 to a factor x7.5 depending on use case conditions.

2. **Connected objects and cars**

- Connect objects in cars: Variability-aware design techniques to improve reliability and yield of next-generation SDR platforms;
- Improved low-power hardware building block for entertainment: a system-on-a-chip (SoC) was developed and succeeded to improve the Performance/Power ratio by a factor x5;
- 13MPIX Sensor with digital CDS readout: to improve frame ratio in order to reduce power consumption and die area for advanced imaging technology. The demonstrator succeeded to highlight the improvement of the Performance/Power ratio by a factor x5.

3. **Health care**

Energy-efficient platform for health monitoring applications: integrated platform for efficient processing of biomedical signals, and addressing technological challenges, such as excessive process variability, energy transfer and power management. This demonstrator succeeded to improve the Performance/Power ratio by a factor x4.

4. **Space**

Reliable multi-core digital signal processor (DSP) architecture: showed the impact of reliability/fault-tolerance mechanisms in relation to power and scalability. This demonstrator succeeded to improve the Performance/Power ratio by a factor x8.

5. **Advanced energy efficiency**

- Ultra-wide voltage range DSP in fully depleted silicon on insulator (FDSOI) process technology: delivers benefits of reduced silicon geometries for high-energy efficiency. Those techniques succeeded to improve the Performance/Power ratio by a factor x2 to x40 depending on use case conditions;
- Low-power radio frequency front-end component: tunable wide-frequency range bandpass filter from GSM to LTE mobile network technologies. This demonstrator succeeded to improve the Performance/Power ratio by a factor x5.

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Health and aging society
- Energy efficiency
- Digital lifestyle
- Design technology
- Process development

PARTNERS

STM-Gnb
STM-Alps
STM-Crolles
Ericsson
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Atrenta
Thales - TCS
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IPCB
IT-PT
IMEC

COUNTRIES INVOLVED

France
Netherlands
Portugal

PROJECT LEADER

Armand Castillejo
STMicroelectronics

KEY PROJECT DATES

1 January 2013 - 30 June 2016

- Energy-efficient heterogeneous many-cores for smart camera: the demonstrator succeeded to improve the Performance/Power ratio by a factor x2 to x25 depending on use case conditions;

BENEFIC was a success, based on the technical achievements reached – and even exceeded – by the eight demonstrators. Importantly, there were clear links between the elementary technical bricks used in these demonstrators and the application domains where these technologies were demonstrated, illustrating the benefits of BENEFIC's holistic approach.

The project was also successful in terms of intellectual property (IP) and scientific output, adding value by generating seven patents; 45 scientific publications and posters; and being runner-up for the IET Innovation Awards.

Market share and well-developed, disseminated research

In concrete terms, the project generated significant added-value to the project partners by creating the first and only European DSP intellectual property (IP) in space; and providing various technologies that will give participants a competitive edge in the image sensor market, estimated at 6 billion units in 2018.

The industrial project partners are aiming to increase their footprint in their markets, as well as win market share with innovative and robust products. To achieve all of this, the contribution by BENEFIC's academic partners was essential in the research and development of new technologies, which, in turn, helps these participants fulfil their primary mission: to develop and disseminate knowledge needed to keep European R&D at the cutting-edge.

Benefits to sales and ecology

Thanks to BENEFIC, benefits from energy collection and distribution will be, in general, integrated and these innovations transferred to other energy-constrained domains, where growth of smart mobile-devices will be directly or indirectly affected. This means that BENEFIC's technological advancements in energy will also give other European suppliers a competitive advantage. The market for ground and satellite radios, for example, is estimated at US$1,582m in 2018; and the biggest growth is expected between 2012 and 2015 with the introduction of new SDR systems on the market. The professional radio market is estimated at US$9 billion a year, and equipment volume estimated between 22m-40m units worldwide.

Then there is the Internet of Things (IoT), with increasing opportunities for new mobile devices. A significant increase in connections is envisaged, reaching 350m by 2016. Importantly, delivering digital content with the right user-experience across different devices (digital convergence) is already visible; and large-scale adoption will be possible, thanks to the longer battery life these devices need.

BENEFIC developments also address the many-core market, especially in the space domain, where many actors are developing new applications. Market-size estimates for space-oriented many-cores will exceed €100m in 2016 and could reach up to €800m in 2020. With satellite systems enabled for space use through BENEFIC techniques, this market could be worth €1 billion by 2020.

BENEFIC also impacts advanced R&D in energy efficiency, leading to innovation needed to create the next technological-breakthrough, and ensure competitive advantage and market opportunities. BENEFIC's advances should help industry focus on high-level systems and tools; architectural innovations and design; and efficient technological devices at process level.

BENEFIC will play an important role in helping healthcare move from today's hospital-centric approach, to a more patient-centric one, enabling ubiquitous and pervasive health monitoring. Costs will also be significantly reduced and well-being improved once patients are treated in their own environment. The total size of the medical-devices market in 2011 was estimated to be US$309 billion. And growth will continue to be driven by a global ageing population and the expected increase in the incidence of chronic diseases, particularly in developing countries.

Finally, there is also an environmental spin-off from this project. Energy harvesting creates green energy, thus reducing the use of carbon-based energy (with its environmental hazards). The distribution part of the system must be built to gather the harvested energy when available. This requires the integration of harvesting in the whole process of storing, managing and distributing power.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

CATRENE (E! 4140), the EUREKA Cluster for Application and Technology Research in Europe on NanoElectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

PROJECT RESULTS

CA703

Lower development costs and faster time-to-market expected with Open ESL technologies [OpenES]

This project's objective was to provide the European industries with open electronic system-level design and verification methods and tools. These enhanced system-level design capabilities increase productivity, reduce system design costs and increase product quality, thereby improving competitiveness of European semiconductor and system-design companies.

Building on Europe's strengths in integrating advanced complex systems is important to its competitiveness. And as demand for more features and improved functionality is making systems design and development more complex, there is an increasing need for advanced methods and tools to improve productivity (faster time-to-market) and quality (less design errors and less re-designs) in system-level design and verification in order to allow European industries to remain competitive. Electronic design automation (EDA), which involves a diverse set of software algorithms and applications, aids the designing of complex, next-generation semiconductor and electronics products, which is where OpenES plays an important role.

ESL and open standards improve chances of success

True to its name, OpenES developed a solution based on open standards and on a methodology called electronic system-level design and verification (or ESL), which makes use of appropriate abstractions in order to increase comprehension about a system, and also increase its chances of a successful and cost-effective implementation.

In particular, this methodology:

- Fills in gaps in design-flows with new interoperable tools and/or improve existing tools/flows ensuring the semantic continuity of the design flow;
- Specifically focuses on integral support of both, functional and extra-functional requirements – from specification to verification – jointly, with the use cases defined at system level;
- Raises reuse capabilities from intellectual property (IP) to hardware/software (HW/SW) subsystems in order to eliminate integration effort by supporting reuse of pre-integrated and pre-verified subsystems;
- Enhances interoperability of models and tools by upgrading and extending existing relatively new open standards (SystemC TLM, SystemC-AMS, IP-XACT).

Key project activities included:

- Implementing the OpenES Modelling Kit;
- Defining IP-XACT extensions for extra-functional properties and provide interfacing solutions for models and tool flows;
- Defining common requirement traceability flow for functional and extra functional (timing, power and thermal) verification, starting at high abstraction-levels (UML);
- Implementing case studies and evaluating OpenES design-flow performances;
- Promoting the project globally and sharing relevant information.

Notably, OpenES achieved the following:

- All 29 technical deliverables have been released;
- Six milestones have been successfully reached;
- Benefits to OpenES technologies have been quantitatively measured in five case studies, showing up to 33% in manpower savings;
- Joint standardisation actions have been undertaken, resulting in a significant European impact by defining new standards;
- Several new tools or updates have been implemented and are now available for commercial use, expanding market opportunities for several project partners;

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Design technology

PARTNERS

CISC Semiconductor GmbH
Docea/Intel
ECSI
Magillem Design Services
STMicroelectronics
Thales Communication & Security
Thales Research & Technology
NXP Semiconductors N.V.
Synopsys
Vector Fabrics
CEA LIST
UGA-VERIMAG
Technische Universiteit Eindhoven (TUE)

COUNTRIES INVOLVED

- Austria
- France
- The Netherlands

PROJECT LEADER

Laurent Maillet-Contoz
STMicroelectronics

KEY PROJECT DATES

1 April 2013 - 31 August 2016

- A global dissemination effort has spread the project results in Europe and in the US, reaching American and Asian communities. This effort produced:
  - 21 scientific papers
  - 25 presentations at workshops and seminars
  - 15 exhibitions and demonstrations
  - Four new courses/training materials

Lower development costs and faster time-to-market

The common open and extensible solutions developed are providing a design framework and interfaces built on standards wherever possible. Extensions of standards have been initiated where necessary. Thanks to this openness and the use of standards, every project partner can achieve an advanced and complete system design-flow, enhancing it according to specific requirements from a given application domain. This offers significant improvements in system-design capabilities and a good cooperation between integrated circuit/intellectual property (IC/IP) provider and system integrator. The broad relevance and functional capability of this common approach are demonstrated through case studies from various key domains of European industry: wireless/software defined radio; multimedia/set-top-box; automotive/traffic and security; and industrial/power control. Final results of the case studies have proven the relevance of the approach deployed, and confirm the benefits of the technologies developed in the project.

OpenES will also maintain state-of-the-art technology at universities and research institutes, ensuring high education standards. It will also impact European industry in two ways. Firstly, it will enhance the system-level design to reduce development costs by improving the co-operation between system houses and semiconductor companies; and by establishing an ecosystem based on open standards to create high-level models and associated tools, thus avoiding expensive development of in-house, proprietary approaches and tools.

And secondly, OpenES will optimise products to increase competiveness by innovating product architectures and increasing efficiency in product design, with less redesigns, reduced system-development cost and faster time-to-market. Furthermore, it will increase Europe's heterogeneous and embedded systems in a more optimised and systematic manner. Together, it will maintain Europe's leading position in product innovation and design in major applications.

Increasing role of ESL will drive the EDA market

The EDA market grew 9% in 2010 and 14% in 2011, reaching US$4.19 billion worldwide in license and maintenance revenue last year (excluding services and IP). The sector employed more than 26,000 people at the start of 2012. A steady 10% growth rate is predicted for the next five years, sustained by a continuous shift of design methodology to the ESL level. And the increasing role of ESL in overall IC design flow is indeed expected to foster the market for new dedicated EDA tools.

Notably, according to market intelligence, 2014 marked the first year of really solid growth for ESL tools in the EDA market. ESL technologies started experiencing their long-awaited user adoption in earnest. For the first time, ESL growth was higher than that of either the downstream computer-aided engineering market or the EDA market as a whole.

Finally, there is also good news on the IP and subsystems market fronts, where development costs of a single system-on-chip (SoC) is over US$85m and this cost is rising rapidly. Encouragingly, the industry has responded to these rising costs through the concept of IP blocks: functional components that act as building blocks which can be integrated into a SoC. The SoC market is expected to grow from $85.9 billion in 2011 to $117.8 billion in 2016, at a CAGR of 6.47% from 2011 to 2016.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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PROJECT RESULTS

CT315

Using creative packaging of power-drive electronics in electric vehicles to reduce costs while increasing reliability and efficiency

[EmPower]

EmPower developed an innovative packaging concept for e-mobility and industrial applications, especially in automotive, resulting in a drastic improvement in heat dissipation and thermal impedance of embedded power modules, which can lead to other technical, business and financial benefits.

Packaging power-drive electronics – such as inverters, battery chargers and power controllers – in electric vehicle (EV) engines operating in harsh conditions, is based on costly direct copper-bonded (DCB) ceramics. However, deploying an embedded power-module offers an excellent way to reduce size and weight of power-drive electronics in EVs, while increasing switching performance and improving heat management.

Developing a total power-drive packaging concept

The EmPower project developed a total packaging concept for power-drive electronics in EV engines, based on embedding power-drive components as thinned chips into a built-up glass-fibre reinforced epoxy-resin layer. This creates large-area interconnections to form a conductor structure with the lowest possible thermal impedance needed to achieve optimal heat dissipation. In addition, it embeds the power semiconductors in a module which offers heat removal on both sides over the shortest possible heat-conduction paths.

This embedding technology also sets aside thick wire bonding of power devices on DCB substrates. Now, interconnections between these power devices and wire bonds are a primary source of parasitic inductances in today's power packages. This leads to significant switching losses and critical shortcomings (like limited lifetime and reliability issues due to high power-loss density). On the other hand, EmPower's packaging concept contains copper interconnections (with large cross-sections) between the power devices and the package pads by short copper-filled via and large copper cross-section. This technology enables the necessary copper connections and pads to be placed on both sides of the package in an arbitrary manner, thus satisfying the needs for both, high-electrical and high-thermal conductivities.

The entire development and manufacturing of such power cores takes place in a state-of-the-art PCB manufacturing environment. The full production capacity using large 18"x24" panels will achieve cost reduction by economy-of-scale manufacturing. In this context, the EmPower concept sets unusual demands on device metallisation, comparable to copper-electroplating processes, and the development of cost-effective thermal management solutions based on thick-copper interconnections and thermally conductive, electrically isolating materials.

The project also developed three demonstrators and ran simulations, with very promising results:

- A 50W demonstrator with a double-diode rectifier with the footprint of a D2PAK and a height of a tenth of this package. This ultra-thin power package passed all tests;
- A 500W demonstrator with a DC-AC converter for a pedelec application, formed by a B6 bridge with MOSFETs and a logic module. This module passed all major tests and showed excellent switching properties;
- 50kW demonstrator with a DC-AC inverter for EVs using IGBTs and diodes. It was able to demonstrate the interconnection concept and its reliability and thermal characterisation.

Supply-chain structure

Now, during the project set-up phase and initial analysis of target applications for the automotive industry, it became clear that expertise would be needed at the silicon-component level, as well as for embedding large and thin power components; in interconnection technology for building the power modules, and in modifying power applications to demonstrate the benefits of the newly developed power packages and power modules.

And the project consortium represented major stakeholders in the EV value-chain with financial interest in the production of compact, power-efficient embedded cores and modules which can improve the electric motor's autonomy thereby inducing energy savings; increased long-

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Energy efficiency
- Digital lifestyle

PARTNERS

AT&S
Atotech
Conti
STMicroelectronics
ILFA
Institute TU Berlin
University TU Wien

COUNTRIES INVOLVED

- Austria
- Germany
- France

PROJECT LEADER

Johannes Stahr
AT&S

KEY PROJECT DATES

01 May 2013 - 28 February 2017

term stability and reliability; and environmental friendliness. The project consortium was therefore organised as a supply chain to handle the technological gaps and challenges in developing embedded power-modules and power packages.

Technical, financial and ecological impact

Notably, EmPower generates technical, financial and ecological benefits. Two key project results – double-sided cooling and conductivity of semiconductor switches without the use of bond wires – enables a drive to be mounted directly on the motor to form a single unit with the motor housing. It will lead to lower power-resistivity and inductance of the power switch, and also provide a wider switching-frequency range and high power-efficiency. EmPower technology also promises to reduce the volume of the electrical control unit (ECU) of the drive inverter found in EVs and hybrid electrical vehicles (HEVs), thus lowering space requirements In such applications. This is critical because package density, weight and power-losses are the most design-critical boundary conditions, especially in the cooling system.

Of course, the general health of the automotive business, the main beneficiary of EmPower, is also crucial to the success of this project. Encouragingly, we see that automotive has the second-highest compounded annual growth rate (CAGR) at 14% in 2016. The innovative packaging of power-drive electronics of EV engines (and in some cases consumer applications) will result in lower costs and higher reliability, and therefore secure a competitive-edge in the European automotive industry. Analysis of the value-chain of existing power modules underscores future importance and ubiquity of the power module developed in the project, with roughly 25 % of the value-chain benefiting from the new power-module concept. Within automotive, EmPower's main potential market is EVs. Here, car registration is expected to rise from 500,000 in 2015 to over 1m in 2020. Importantly, power modules are not limited to only the electro-mobility sector: power semiconductors, excitation designs and mechatronic integration are also needed for industry and the consumer market.

And on the ecological side, a key success factor will be to develop power-efficient energy converters in order to maximise CO2 reduction in the face of increased individual mobility. EmPower is doing its bit in this area. A European industrial consortium (which includes an EmPower project partner) is already involved in developing high-end green and efficient technologies based on this project's findings and deliverables. Certainly, a win in the sustainability battle.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

CALL 6

PROJECT RESULTS

CA114

Non-galvanic wireless connectors impact cost and efficiency in autonomous cars and the Industrial Ethernet [WiCon]

WiCon developed and demonstrated low-cost, highly-integrated electronic systems for data and power transfer. Importantly, they can also replace the troublesome galvanic connectors in the consumer and industrial market segments.

Galvanic connectors (such as USB cables used to connect peripheral devices, like printers, to the PC) are widely deployed in electronic systems. However, these types of connectors come with several key disadvantages:

- Prone to wear and tear leading to functional failure in consumer electronics and in professional systems;
- Connectors for high-speed links increase the cost of the system considerably;
- Reliability problems, such as with SD memory cards which get damaged due to mechanical stress;
- Connectors in professional applications tend to get dirty and/or break after a limited operational time, increasing machine down-time and maintenance cost;
- Physical connectors may limit the operational design freedom in industrial production lines, such as conveyor-belt systems.

Fortunately, advanced CMOS (complementary metal oxide semiconductor, a technology used to produce integrated circuits), enables a new kind of wireline communication which can be deployed to resolve these issues.

Smart mmWave solution for data and power transfer

Semiconductor technology scaling has enabled low-cost CMOS circuits to operate in the mm-wave frequency range (30 to 300GHz) where large bandwidths are available. These bandwidths are exploited in radar applications (automotive at 77GHz) and in high-data rate wireless communications (such as point-to-point link and new 5G radio interface).

Crucially, advanced CMOS also enables a new kind of wireline communication which has two main advantages:

- The “wire” is simply a plastic fibre or hollow tube, which is much lower in cost and weight compared to co-axial, copper-based cabling;
- The coupling of the mm-wave from the CMOS chip into the fibre does not require complex heterogeneous semiconductor implementation, as is the case in optical fibre links.

Based on this advanced technology, the WiCon project developed low-cost, highly-integrated system solutions for galvanic connector’s replacement in the automotive and industrial market segments. Smart electronic systems for data and power transfer were demonstrated, exploiting ultra-low-power point-to-point mmWave connections and optimised power-transfer technologies, merging near-field communication (NFC) with wireless-charging applications.

Wicon’s main focus areas were:

- A high-data-rate radio frequency (RF) link, such as mmWave, for bi-directional multi-Gbps data-transfer capability;
- An NFC link for interchange of security keys and identification codes, and to set up initial (control) data exchange between base-unit and contactless-unit;
- Wired data interface (such as 10Gbps USB and Ethernet 1G) to extract the data from the wired cable and forward it on the high-data-rate RF channel. At the other end, it will receive the bits from the high-data-rate RF channel and transmit them in a way compliant with next-generation wired standards (like 10Gbps USB and others).

In addition, there were demonstrations of polymer waveguides carrying mmWave signals for data-transfer rates above 10 Gbps (gigabits per second). Importantly, these can be deployed as low-cost replacements for expensive optical components used in the next-generation 10Gbps USB standard. Considerable progress was also made in realising high-speed wireline communication over polymer fibre demonstrators. Most notably, a prototype operated at 140GHz exhibiting 10Gbps data rate. And the building blocks for another prototype operating at 80 GHz, were completed.

PROJECT CONTRIBUTES TO

- Communication
- Energy efficiency
- Digital lifestyle

PARTNERS

KU-Leuven
NXP Belgium
NXP Netherlands
TE Connectivity
TU-Delft

COUNTRIES INVOLVED

- Belgium
- Netherlands

PROJECT LEADER

Joost van Beek
NXP

KEY PROJECT DATES

01 January 2015 - 31 June 2018

Main project deliverables were:

- Functional requirements for copper cabling replacement in high-speed datacomm;
- Functional demonstration of the high-data-rate links over plastic fibre for Automotive Ethernet and Industry 4.0;
- Polymer mmWave fibre to support high-bandwidth, low attenuation, low dispersion and superior electromagnetic interference (EMI) compliance;
- High-bandwidth 80-120GHz CMOS transceiver integrated circuit (IC) development supporting high data rates;
- mmWave packaging and assembly to connect fibre to transceiver IC;
- Modem to interface the Ethernet physical coding sublayer (PCS) to transceiver IC.

Notably, Ethernet implementations based on mmWave also offer additional benefits over copper: such as electromagnetic immunity, low latency, and environmental resilience (like corrosion), as well as, such advantages as easier field termination, lower weight, and passive contactless, in-line connectivity. In fact, depending on cost, mmWave technology could completely replace traditional copper, significantly increasing mmWave's market potential and 'saleability' of WiCon as a project.

Well-balanced project consortium

The WiCon consortium was a relatively small, but well-balanced, project team comprising a well-known IC manufacturer, whose expertise was complemented by project members from three major European technical universities. These educational institutions, which had excellent track records in electromagnetics-related projects and mmWave circuit design, also co-operated on measurement and characterisation of the polymer waveguide band. Together, these partners had the necessary know-how and production base to turn the emerging technologies of mmWave and polymer waveguides into successful marketable products.

Driving Europe's automotive and industrial sectors

WiCon supports Europe's efforts towards a new class of energy-efficient systems capable of sensing, communicating and actuating in a smart and power-efficient manner. It also reflects the CATRENE programme's vision to develop and deploy communication electronics systems where new technologies and architectures combine adaptability and performances in a novel way.

Importantly, WiCon also secures the competitive power in Europe's two key sectors, where its related products and services can be marketed. The first is automotive, where the driving forces are autonomous and driver-assisted vehicles, in which data-intense technologies are expected to be installed. These include lidar (a detection system which works on the principle of radar but uses light from a laser), GPS, and computer vision. What is more, these applications will further trigger the need to network and distribute that information throughout the vehicle at high data-rates, resulting in a market growth for in-vehicle networks (IVNs) due to increased demand for these data-hungry applications. Reflecting this growth, the annual number of network nodes is expected to increase from 3 billion in 2016 to more than 5 billion in 2022.

The other target market for WiCon is industrial automation, or specifically Industry 4.0 (the fourth industrial revolution), a name given to the current trend of automation and data exchange in manufacturing technologies, including the internet of things (IoT). It incorporates machine learning and big-data technologies to harness the sensor data, machine-to-machine (M2M) communication and automation technologies. However, these trends require that all 'things' are directly IP (internet protocol) addressable, for which Ethernet is the most logical choice. According to Market Research Future, the global industrial Ethernet switch market is expected to reach US$ 2.0 billion during 2017-2023, with a CAGR of 14%. The contributing factors are the adoption of industrial automation and the deployment of the Industrial Ethernet as the preferred networking solution.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

PROJECT RESULTS

CA116

How reduced interference and concurrent communication streams are set to benefit and drive the Internet of Things, gateway devices and mobile networks [CORTIF]

CORTIF ensures that radio spectrum can be used by multiple, concurrent applications without detrimental mutual interference and resulting performance degradation. Finding such a solution is significant when you consider some seven trillion wireless devices will be deployed by 2020. This project will benefit three key domains: professional mobile (with 5G networks); Internet of Things (less interference) and gateways (set-top boxes running multiple communications without interference). Crucially, this project also improved such metrics as throughput, radio frequency standardisation and power consumption.

Coexisting wireless networks suffer significant mutual interference with associated performance degradation. This interference takes the form of time and frequency collisions and becomes a critical problem in achieving reliable wireless communication. Furthermore, interference sources can also be found inside equipment. As end-users become increasingly familiar with mobile devices and heavy bandwidth applications, the available spectrum is becoming cluttered. In addition, coexistence of mobile services on adjacent bands is necessary to extend existing services. However, bandwidth-allocation cannot be guaranteed for extended wireless systems in the SIM bands; while there is pressure for higher data-rates and even greater reliability. In addition, there is the need to support billions of sensor devices which require ultra-low-power radio connections.

Ensuring concurrent use of radio spectrum without mutual interference

The CORTIF project's key response was to address the problem with multiple, concurrent applications operating in the radio spectrum without any detrimental mutual interference. This was applicable, both at the application level (same location), and technology level (same printed board). Project members were assigned tasks based on experience and expertise. Application experts (in mobile and set-top boxes) defined the system requirements and constraints; semiconductor suppliers developed the technical approaches; and integrators created and demonstrated working proof-of-concept level solutions highlighting the achievable improvement considering metrics such as throughput, radio frequency (RF) standardisation and power consumption.

The project delivered these key components:

- An ultra-selective active filter designed to enable the coexistence of a 2.5GHz EMEA LTE system. Proof of concept for a sub-GHz application was conducted and then ported on 40nm for 2.4 GHz operation;
- An anti-interference spectrum-sensing platform algorithm and software-defined radio (SDR) techniques;
- Design of an architecture based on a ↗Σ receiver. This architecture is highly flexible and covers a wide range (up to 6 GHz with a 65 nm CMOS technology);
- A hardware combiner prototype of integrated circuit techniques to remove interference in the analogue domain, considering radio impairment, like delay spread, phase shift and attenuation path;
- A wideband receiver with amplitude-domain filtering based on a nonlinear transfer function;
- The design and production of an antenna that operates in the 3G and 4G spectrum for home devices.

Simulation platforms were also developed and successfully validated for:

- Resource management strategies, such as power usage, bandwidth, and radiation;
- Using game theory for interference avoidance in a Bluetooth low-energy system;
- Coexistence between DVB-T2-Lite and LTE;
- Coexistence between LTE and LAN;
- Coexistence between Wi-Fi and Bluetooth low-energy;
- Digital cancellation of the professional mobile coexistence system, aimed at removing baseband interference in the narrowband received signal;
- Far-field radiation simulation environment for automotive integrated circuit products;
- Simulation models, coexistence methodology and measurements for RF physical layers (DVB-T/T2, LTE-U, WLAN 802.11bgn, ZigBee, Bluetooth);
- Modelling interference between sender/receiver pairs.

PROJECT CONTRIBUTES TO

- Communication
- Energy efficiency
- Digital lifestyle
- Design technology

PARTNERS

BUT - Brno University of Technology
Airbus Defence and Space Systems
GS LDA
IMA - Institut mikroelektronickych aplikaci
IMEC
IMT - Institut Mines-Telecom
UPC - Universitat Politecnica de Catalun
IT - Instituto de Telecomunicações
NXP France
NXP Netherlands
Technicolor
Technolution
TUE - Technical University Eindhoven
XLIM

COUNTRIES INVOLVED

- France
- Portugal
- Czech Republic
- The Netherlands
- Spain

PROJECT LEADER

Dominique Defossez
NXP

KEY PROJECT DATES

01 July 2014 - 30 June 2017

Other project achievements include:

- A compact gateway which enables concurrent wireless systems, including 3G/4G networks and 802.11ac radios;
- Reliable communication for ISM 2.4 GHz for low-power, wireless devices in the healthcare domain;
- The development of a substrate extraction to handle wafer-flow (for EMC), and noise-coupling analysis (in automotive integrated-circuit applications).

Successful European collaboration

A good working environment produced effective project co-operation, creating trust among intellectual-property suppliers, integrated-circuit manufacturers and application owners. This was helpful in approaching coexistence techniques from different angles, but it also created a better understanding of coexistence constraints. In addition to its technical achievements, CORTIF also generated nine patents and 40 publications.

The impact of the work done by CORTIF is multifaceted and its goals cannot be met just though individual national research programmes, or projects developed by a single company. The scope of the project makes pan-European collaboration and the participation of 14 key European players from industry, research and academia in critical areas of CORTIF indispensable.

Impacting Europe and benefiting project partners

The three domains addressed by CORTIF will benefit from:

- Interference reduction between IoT devices;
- Set-top box capacity to run several wireless communications simultaneously in the same room with limited interference;
- Optimised spectrum usage for 5G emergence.

Expectations are also high for CORTIF's own industrial project partners, especially with:

- New IoT multi-standard devices expected to make a breakthrough;
- A new airline private mobile-radio secured against LTE-based broadband systems;
- A Bluetooth low-energy communication interface immune from the ISM band;
- Electronic design automation (EDA) tools expected to be deployed worldwide;
- A set-top box which supports seven concurrent wireless signals;
- A flexible radio test and characterization platform (FRaTaC), which optimises RF designs for operation in a busier RF spectrum;

Project achievements also had a wider impact, such as improving data-transfer reliability and signal range, which in turn strengthened European manufacturers' position in their market, and accelerated the business ramp-up of new wireless products. Furthermore, by supporting the coexistence of wireless communications through IoT, set-top boxes, TV tuners and professional mobile-radio (markets in which Europe leads), CORTIF consolidated Europe's position in these and other new wireless-service markets.

In addition, by proposing appropriate technical solutions for the coexistence of RF-spectrum sharing, European standardisation bodies will be more flexible in ruling on frequency allocations. It is also important to recognise Europe's competitive advantage: the complete development platform combining network control and drivers (as part of home automation) with increased security. Of course, CORTIF's coexistence techniques offer Europe a crucial advantage, especially over American semiconductor suppliers, its key competitors.

Looming on the horizon

However, there is more work on the horizon following CORTIF's achievements: wireless-communication coexistence will soon face new challenges for higher frequencies. With the emergence of 5G, for example, there will be the need to address coexistence in the millimetre wave bands, and between 5G communication and RF sensors in a confined space, such as in vehicles and airplanes.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

PROJECT RESULTS

CA118

Critical communications deployed in public safety and disaster relief are readied for major upgrades [FITNESS]

FITNESS prepared current European and global mission-critical radio communications (used typically for public safety and disaster relief) for new data applications and features, and the use of smart devices. Crucially, to achieve all of this, radio communication systems needed to move from operating exclusively in the narrowband, to working in a mixed environment of multistandard narrowband and broadband. That was this project's focus.

The public-safety community needs a mission-critical radio network to cover professional mobile radio (PMR) highly secured applications (police, fire services, ambulance), and professional applications (such as utilities, fleet management, factory-site service). Importantly, mission-critical communication fulfils five key requirements demanded by end-users:

1. Resilient and high-availability infrastructure;
2. Reliable communication with an extremely short setup time;
3. End-to-end secure communication with modifiable encryption;
4. Terminal-to-terminal communication support (direct mode);
5. Point-to-multipoint communication support (group communication).

Today, there are more than a thousand mission-critical radio networks in over 120 countries, including public safety networks and those in industrial areas. Voice and data services are currently provided by different digital narrowband PMP technologies – such as TETRA, TETRAPOL and APCO-25 (a suite of standards for public-safety digital mobile radio communications) – which were originally dedicated to voice services and later adjusted for narrow bandwidths (initially used by analogue radio).

While these technologies are very efficient for voice, they are not suitable for data because of limited capabilities and capacity. Finding a solution was imperative because public-safety users need new data applications and features, and also to connect smart devices. Furthermore, there are new system requirements for these communications systems: typically, high availability, interoperability and scalability, together with increased resilience, trustworthiness, efficiency and security.

Now, an enhanced version of TETRA called TEDS (TETRA Enhanced Data Service) was initially deployed to provide wideband data services and to improve the data rate. However, a much better solution makes use of the long term evolution (LTE) standard deployed in wireless broadband communication for mobile devices and data terminals. But this meant technical challenges involved in moving from an exclusive narrowband operating environment, to a mixed narrowband-broadband one.

Low-cost and versatile PMR multi-standard platform

FITNESS researched and developed a low-cost and versatile PMR multi-standard platform (narrowband; and LTE for PMR broadband) with additional PMR-dedicated functionality for geolocation. The project also involved important advanced research in architecture, processes and techniques. A case in point is the use of envelope tracking in designing radio-frequency amplifiers to ensure the highest efficiency. Importantly, a key project goal was to have all critical components integrated in a single 3D platform.

Project deliverables included:

- For narrowband: 5 demo-boards for components test; 3 CMOS chips and 1 demonstrator;
- For broadband: 12 demo-boards for components test; 4 SOI chips; 8 SIPs; 5 (BI) CMOS chips and 5 demonstrators;
- For geolocation: 4 demo-boards for components test; 2 (BI)CMOS chips; and 1 demonstrator.

Key project activities involved:

- Investigating an innovative architecture for a CMOS low-cost, narrowband, multi-standard PMR chip. This IC is a transceiver, fully compliant with all existing narrowband PMR standards (TETRAPOL, TETRA (1 & 2), TEDS and APCO-25, and which addresses both 400 MHz and 800 MHz bands;
- Validating the design of critical building blocks and their system re-configurability through the demonstrators of standalone test-chips;

PROJECT CONTRIBUTES TO

- Communication
- Safety and security
- Energy efficiency
- Digital lifestyle
- Design technology

PARTNERS

Airbus Defence & Space
NXP Semiconductors
BeSpoon
Mikroelektronik (MKR-IC)
CEA-Leti
IMS Bordeaux
ISEP Paris
Telecom Bretagne

COUNTRIES INVOLVED

France
Turkey

PROJECT LEADER

Sami Aissa
Airbus

KEY PROJECT DATES

January 01, 2015 - December 31, 2018

- Studying power-efficiency improvements through envelope tracking;
- Designing a high-power, reconfigurable CMOS power amplifier (PA) compatible with envelope-tracking power efficiency;
- Integrating a radio frequency (RF) transceiver and a high power reconfigurable CMOS PA fully compliant with long-term evolution (LTE) broadband and PMR standards, addressing both 400 MHz and 700 MHz bands;
- Developing a technique for 'tuning' the radio antenna to ensure maximum efficiency over a range of frequencies;
- Integrating the chipset that handles indoor and outdoor positioning;
- Designing a 3D platform which combines heterogeneous technologies that allow high-level integration of different systems-on-chip (SoCs) dedicated to PMR in a single, low-cost system-in-package (SiP).

Towards closer collaboration

FITNESS partners actively participated in the ETSI and 3GPP standardisation bodies, and in some 30 workshops, forums, symposiums and conferences. These were prime events to promote the project, but also disseminate knowledge gained. This knowledge included such areas as RF specifications, multi-standards architecture, frequency bands, innovations in CMOS and SOI processes, and packaging. What is more, thanks to FITNESS, there is now a real opportunity to cross national boundaries and create the critical mass needed to move from the current approach of using a mix of integrated circuits and discrete components, to proper chip integration. Notably, all of this requires investment and cooperation between European industry and educational and research institutions.

European societal, business and financial benefits

FITNESS will provide Europe's emergency services with state-of-the-art communications. By developing PMR broadband capability while preserving backwards compatibility and allowing new interoperability with existing narrowband PMR systems, FITNESS will help meet public-safety communities' requirements. It does this by supporting the European effort to deploy next-generation PMR wireless applications and improve the capacity, security and efficiency of mission-critical services, such as police, fire and ambulance.

There are also business and financial spin-offs. According to Markets & Markets, a research company, the public safety and security market size was valued at US$ 247.55 billion in 2016 and is projected to reach US$ 532.39 billion by 2022, at a compound annual growth rate (CAGR) of 14.0%. The deployment of broadband technology and the know-how of products in the US 700 MHz band, as well as in the European 400MHz band, creates an opportunity for European companies to further improve their business and also secure a competitive advantage.

European leadership potential

And finally, there is European interest in the geolocation function (featured in FITNESS) in connection with the smart-manufacturing initiative, Industry 4.0. This project will deliver the very first radio to deploy indoor and outdoor geolocation, providing European emergency services with state-of-the-art locating functionality, combined with extended operational ranges. This is a unique occasion for Europe to build a leadership position in precise indoor-location systems, an area that was first pioneered by US players with solutions that are now expensive and not integrated enough to address the challenges of the current market.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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PROJECT RESULTS

CT217 | Reliability and adaptivity essential for building resilient integrated electronic systems for automotive and avionics [RESIST]

Focusing primarily on reliability and adaptivity of electronic systems for the automotive and avionics industries, the RESIST project developed design methods and solutions that will be dependable and resilient to intrinsic and extrinsic failures in future process technologies.

An increasing sophistication and complexity of systems found in vehicles (including electric cars), airplanes and satellites, as well as, their high-performance, light-weight and compact-size requirements, are all placing greater demands on their electronic components. For example, ever-higher integration is pushing the limits of reliability – and thus their operating life – of current devices, particularly in the harsh operating conditions of automotive and avionics applications. This calls for safety-centric, robust systems based on advanced electronics, which can actively and in real-time handle problems, such as system-performance degradation and errors, before they actually cause failures.

Beyond the traditional hardware-design paradigm

The RESIST project developed new design methods for semiconductors and electronic components which are vital for next-generation electronic systems for avionics and automotive applications, with ever-higher demands on reliability, cost-effectiveness and quality of semiconductor devices. Crucially, RESIST looks beyond the traditional hardware-design paradigm of embedded semiconductor-based devices, which assumes that no device will degrade or operate incorrectly during the lifetime of the device.

RESIST's objectives were to:

- Enhance the lifetime of embedded devices, from today's 10-15 years, to tomorrow's 25 years for automotive, and 35 years for avionics, with a reliability indicator of maximum 10 failures-in-time (FIT) for avionics;
- Enable an innovative 'design for resilience' approach for embedded devices that is at least twice as cost-effective as conventional redundancy practices for the same level of system reliability;
- Increase by at least 20%, the number of integrated components, or integration density of such components, for integrated electronics systems in cars and airplanes for the same, or higher, level of system reliability;
- Reduce reliability-testing costs by 25%, and reduce the qualification time by 30% for integrated electronic-components;
- Develop an early-warning system which monitors the condition of critical components in safety-critical applications.

On target, RESIST achieved all nine milestones and 23 deliverables according to plan.

Among the deliverables were proof-of-concept demonstrators for automotive and avionic applications, where key features and benefits are:

- Highly efficient and a reliable driver for electro-motors usable in electrical vehicles or safety-critical applications, like electrical steering;
- Self-healing and self-regulating processors exploiting time redundancy;
- Resilience and 'health'-monitoring of safety-critical automotive networking applications;
- Good average testing tool that cleverly identifies good circuits for aerospace applications.

Other notable achievements

RESIST designed and developed state-of-the-art IPs, models and tools at a component and system level. All of this was achieved by co-operating vertically with the entire value chain, and across country borders. The consortium also helped promote the project and its deliverables, and disseminate the knowledge it gained, through some 130 contributions to conferences, papers, workshops and the like, including nine talks, and 13 PhD and 11 Master theses. RESIST also (actively) supported standards through its involvement

PROJECT CONTRIBUTES TO

- Automotive and transport
- Safety and security
- Design technology

PARTNERS

NXP-NL (project leader)
ATMEL Nantes SAS
BOSCH
Airbus
Nexperia
Heliox
Infineon
IROC
MunEDA
NXP-D
ST-FR-CRO
Volkswagen AG
CEA-LIST
Fraunhofer IIS/EAS
Institut Polytechnique de Grenoble
ISEN Toulon
Reutlingen University
Technical University Delft
Technical University Eindhoven
Technical University Munich
University of Bremen

COUNTRIES INVOLVED

- The Netherlands
- France
- Germany

PROJECT LEADER

Pierre-Marie Dell'Accio
NXP

www. resist-catreneproject.eu/homepage

KEY PROJECT DATES

01 September 2014 - 31 December 2017

in four standardisation working groups (ISO26262), as well as its collaboration with the CMC, AEC and JEDEC standardisation organisations.

Targeting European automotive and avionics markets

Importantly, European automotive and avionics industries rely on the performance, reliability and longevity of electronic systems for their success and to ensure the quality of their products and solutions. The automotive and avionics markets were estimated in 2016 at € 289 billion and € 320 billion, respectively. However, ia growing penetration in electric vehicles (EVs) and hybrid vehicles (HEVs) is expected to increase automotive electronic-component demand. Important application segments include safety, advanced driver-assistance systems (ADAS) and powertrains, as well as, infotainment and body electronics.

Crucially, in order to curb the number of fatalities from road accidents, regulatory boards in several countries have taken steps to install safety devices in vehicles. Trends suggest that the greatest growth through 2020 will occur within the safety segment. By 2025, 6.2m vehicles are expected to have automated features. Most OEMs are focused on offering semi-automated features in their cars by 2016 and highly-automated driving by 2021. Within the safety category, collision-warning systems are expected to have a compound annual growth rate (CAGR) of 22% between 2015 and 2020, when sales will reach US$4.1 billion. Looking at long-term developments after 2020, continued growth in the engine-control segment is expected. This will include e-motors and power electronics, as well as, growth in integrated systems and solutions, such as engine-control units (ECUs) for fusion sensors and integrated-control systems that will enable level 4 autonomous driving.

RESIST's work in reliability and resiliency – key enablers in the automotive and avionics industries – will further increase the chance of success for European automotive suppliers and manufacturers. This is because RESIST's developments demonstrate fail-safe technologies that not only contribute to reducing the number of (road) accidents; but also in securing European leadership in an extremely competitive sector, where recalls are a constant threat to car manufacturers. Of course, there is still room for improvement and advancement. Further R&D work in the form of follow-up projects and industrial collaboration is just what is now needed.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

Cluster for Application and Technology Research in Europe on NanoElectronics

PROJECT RESULTS

CA208

Comprehensive toolset provides mobile devices and mobile internet with enhanced security and privacy protection [MobiTrust]

The next explosion of mobile devices (smartphones and tablets) and mobile-internet users will only make long-standing concerns over privacy, fraud, and security even more urgent. MobiTrust addressed these issues by developing a total framework containing elements that provide current and future mobile platforms with the necessary protection.

The last decade has seen smartphones and tablets became the preferred repository of personal and professional data. We are also witnessing a significant increase in mobile devices (smartphones and tablets) and mobile devices connected to the internet, a trend expected to continue. According to Statista, a statistics portal, mobile internet usage is affecting the daily life of smartphone and tablet users, enabling consumers to access and share information while on the go. There are signs of a promising future for mobile internet usage as global mobile-data traffic is projected to increase nearly sevenfold between 2016 and 2021. According to January 2018 data, the global mobile population stood at 3.7 billion unique users. And as of February 2017, mobile devices accounted for 49.7% of web page views worldwide. This means that mobile devices will be even more exposed to massive attacks (such as botnets, Trojan horses and viruses), as well as illegitimate piracy activities which are increasingly managed and organised in ways similar to sophisticated, legitimate businesses.

Crucially, this raises key technological and societal issues:

- Privacy protection: More and more users are concerned that they lack proper control over their personal data or assets in mobile environments. Little effort has been made to define guidelines;
- Mobile fraud: The global shift of interest from hacker and pirate communities and organisations is putting a higher risk on some high value-added businesses;
- Protection of vulnerable users: The mobile ecosystem is increasingly facing the same problems as the classical internet world, with the development of illegal or criminal activities such as violence and pornography. Little protection in the mobile environment is available for minors and other vulnerable users;
- New trust models and spaces for mobility: Trusted service managers are just emerging, but consumers lack the confidence to perform high-value transactions because these trusted third-parties do not address the mobility, simplicity and confidence requirements which end-users are seeking. Certification or official marks, such as labels, will help.

Building comprehensive mobile defences

Addressing these key issues, the main goal of MobiTrust was to develop a complete framework—including HW/SW (hardware/software) embedded bricks; remote credential lifecycle management tools; judiciary-proof HW/SW forensics tools—aimed at enhancing the security and privacy-protection of future mobile platforms (including smartphones and tablets) with a focus on ARM/Android kernel technology, but also covering more closed environments, such as Apple's iOS.

MobiTrust delivered complete mobile platforms which were based on commercially available off-the-shelf ones in which the project results are integrated in several scenarios. Importantly, existing certification methodology frameworks were extended accordingly to handle such concepts as privacy, compositional security and forensics, which were introduced in the project. These platforms were deployed as demonstrators aimed at validating their security and privacy-protecting nature, as well as their simplicity of use and ease of integration.

MobiTrust demonstrated more than eight security and privacy-protection scenarios, including:

- A fully integrated, real-life simulation of a firefighting-unit's command & control centre deploying technology bricks from the MobiTrust security framework. This scenario also demonstrated the use of private mobile radio (PMR) over LTE (long term evolution), a 4G mobile communications standard;
- BYOD (bring your own device, referring to company policy of permitting employees to bring personally owned devices to their workplace, and to use those devices for work;
- Using a mobile device as a PC to improve end-user mobility and security;
- Performing the necessary security checks to perform a qualified signature on documents stored a mobile device;
- New hardware to improve security and performance of mobile transactions;
- An open source device-management system and an improved secure mobile operating system.

PROJECT CONTRIBUTES TO

- Safety and security
- Digital lifestyle
- More than Moore

PARTNERS

Gemalto
Teclib'
Cassidian Cybersecurity
Cryptolog
NXP Semiconductors
Trustonic
Trusted Labs
OneSource
Commissariat à l'Energie Atomique et aux Energies Alternatives
Instituto de Telecomunicações Aveiro
Instituto Politécnico de Castelo Branco

COUNTRIES INVOLVED


France


Portugal

PROJECT LEADER

Christian Dietrich
Gemalto

http://mobitrust.av.it.pt/

KEY PROJECT DATES

01 December 2014 - 30 November 2017

How MobiTrust will impact Europe

MobiTrust is expected to deliver key benefits in the following areas:

- European approach: MobiTrust participated in developing European mobile-technology bricks that led to several product and solution launches. It is commonly understood that mobile devices' high-end features are mostly developed outside Europe. Significantly, this European project has demonstrated how major elements of security technology can be designed and produced by European companies. The project will also be key to the development of a European approach to mobile security (including privacy-maintenance aspects). And through strong interaction with European initiatives, MobiTrust will also help promote the use of mobile components, thus reducing dependence on off-the shelf mobile products;
- Fraud: With the pervasiveness of IP-based networks for mobile internet, the risk of massive fraud is threatening the economy. This project will help protect critical public and private IT infrastructure from severe financial damage due to piracy and malicious hacker intrusions;
- Protecting critical information: A heavily computerised world is creating new opportunities for the exposure of critical data to malign business-intelligence groups or agencies. MobiTrust will help protect all critical business or intellectual property rights (IPR) of European public or private organisations from widespread disclosure of sensitive information, thanks to a dedicated privacy-maintaining forensics tool-chain;
- European leadership: This project will help Europe maintain its leadership in some high-value business areas—such as mobile/wireless chipsets; multiple secure elements, form factors and enclaves; optical storage and near-field communication (NFC) applications. It will also help European industry take a sound position in all business areas where security requirements are becoming a key concern. This includes building a sound, open SW industry, which will create new products and services. And the worldwide trust module for mobile and other embedded platforms will enable industrial project partners to provide solutions for new market segments and application domains. This, in turn, creates strong market-leadership in trustworthy devices.
- Guarding privacy: Entirely under the control of major European companies, critical technologies developed in MobiTrust should be adopted in an easier way by end-users, considering strict requirements made in the various reference architecture models to protect their privacy. These privacy requirements will be assessed by trusted European certification agencies. In addition, wide adoption of privacy-enhancing practices (PETs) by the security industry is anticipated. Among the expected outcomes of MobiTrust, demonstrating that PETs are in fact easily deployable to improve the experience of end-users, will act as an eye-opener in the mobile security industry, and will create some momentum around the standardisation of PETs.

Finally, a parting thought. With illegal and criminal activities, such as violence and pornography, impeded by MobiTrust, hopefully minors and other vulnerable mobile-users will also feel safer and more protected.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

CALL 7

PROJECT RESULTS

CAT120

Significant improvements in performance and image quality of advanced image-capturing systems [CISTERN]

Better CMOS image sensors, integral design of optics, image-sensor corrections and image processing, as well as high flexibility in multispectral configurations and production volumes, will all lead to improvements in performance and image quality of advanced image-capturing systems. These systems include high-resolution/highly-sensitive security cameras, as well as hyper-spectral, broadcast and time-of-flight ones.

The broadcast market is moving towards the next video standard, UHDTV (ultra-high definition television), for which two generations have been defined (level 1 for 4K horizontal resolution; level 2 for 8K horizontal resolution). In addition, high-end security HDTV is available today and the UHDTV version is expected in the coming years. However, as depth-imaging applications evolve, there are also growing needs to meet higher specifications in features and performance.

Addressing next-generation imaging-application requirements

CISTERN's research & development work covered such technologies as CMOS image sensors, time-of-flight (ToF) sensors, zoom optics, multispectral imaging and real-time image-processing algorithms, all of which are needed in the next generation of the following application domains:

- Digital lifestyle: broadcast image systems for first-generation UHD-TV and 3D entertainment systems;
- High-end security: UHD surveillance systems;
- Multispectral imaging for specific applications, like sorting in the food industry.

CISTERN met all its key project objectives, in particular to:

- Start in-house CMOS image-sensor development. at Grass Valley;
- Develop next-generation CMOS image-sensors with improved pixels;
- Develop high-speed real-time image processing techniques for bigger and faster sensors and improved image quality;
- Develop capability to produce multispectral imagers through hybridisation of multispectral filter arrays on top of CMOS sensors;
- Demonstrate improved performance of CMOS imagers, combined with related processing in a number of demonstrators;
- Demonstrate the readout performance of the CMOS ToF sensor;
- Develop and demonstrate a camera lens assembly with digital chromatic-lens aberration corrections to improve image quality for security applications;
- Deliver demonstrators of the new technologies developed, which will not only lead to manufacturing partners producing new revenue generating products; but also intellectual property in the form of patents and innovative new technologies.

Importantly, the project consortium comprised three state-of-the-art manufacturers in application domains relevant to the project, and two universities with departments specialising in the relevant research areas.

From improved performance to high flexibility

CISTERN delivered the following key benefits:

- An advanced ToF-sensor design with improved performance (better and more CMOS pixels) that makes sorting and mapping functions – increasingly required to improve production quality and productivity in the food industry and modern agriculture – low-cost and also execute faster and more reliably;
- Smaller, high-performance pixels integrated with high-quality optics and image processing;
- In-pixel attenuation functionality and in-pixel area temperature sensing;
- Combined optimisation of a low-cost lens, high-resolution CMOS sensor and high-speed image improvement algorithms inside the camera for best-in-class performance, while lowering the overall cost of the system;
- A high-performance 320k ToF imager, providing four times more lateral resolution and increased depth resolution;
- A new technology offering multispectral sensors through the hybridisation of a CMOS sensor and multispectral filter at pixel scale. This technology offers high flexibility in multispectral configurations and production volumes.

PROJECT CONTRIBUTES TO

- Communication
- Health and aging society
- Safety and security
- Energy efficiency
- Digital lifestyle
- Design technology
- Sensors and actuators
- Process development

PARTNERS

Grass Valley
Adimec
SoftKinetic Sensors NV
Delft University of Technology
University of Burgundy

COUNTRIES INVOLVED

- Netherlands
- Belgium
- France

PROJECT LEADER

Klaas Jan Damstra
Grass Valley

www.cistern.nl

KEY PROJECT DATES

1 April 2015 - 30 June 2018

Markets to match demand

CISTERN's deliverables fit nicely with key trends and developments of several important markets and application areas. For example, broadcast, security & surveillance, ToF technology, entertainment and the food sorting markets all underscore the importance of CMOS, ToF and multi/hyper-spectral sensor technologies across multiple segments. The penetration of CMOS image-sensors is in almost every technology-related market. The mobile market is key to the CMOS image-sensor (CIS) industry. This sector has maintained a 10.5% CAGR between 2016 and 2022 due to the introduction of dual and 3D cameras. General trends in 3D (stacking) technologies are focused on quality, size, weight, cost and robustness.

However, the primary influence on the CISTERN project is the accelerated adoption-rate of UHDTV in broadcast and security; ToF technology in entertainment applications; and multi/hyper-spectral technology in the agriculture domain. In the broadcast market, all camera manufactures launched 4K UHD broadcast cameras and some important ones also took the next step with 8K UHD versions. These cameras are ready for HDR (high dynamic range) productions and make use of the wide colour gamut BT2020. The Olympic Games in Tokyo in 2020 will be the first big event where 8K UHD will be deployed.

In the high-end security domain, we see high-end security cameras, supporting 4K UHD, and thus becoming more accepted in this market. Currently, 4K UHD cameras are, being used in long-range security & detection systems in vehicles for autonomous-driving. Sensors supporting 8K resolutions are now coming to market, but the move to 8K UHD will be slower in this application domain than in the broadcast one. The largest sensor manufacturer in this application space sees significant growth in the mid- to long-term in the image-sensor business. And given this growing market, this manufacturer views surveillance cameras as a new image-sensor application for which it has high expectations.

In addition, according to the latest market analysis, Variant Market Research reports that the forecast for the global gesture-recognition market for consumer electronics is expected to reach $43.6 billion by 2024, with a compound annual growth rate (CAGR) of 16.2% from 2016 to 2024. And sales in the drone market are expected to increase by 25%, as in previous years.

Finally, the hyperspectral-imaging (HSI) sector is also flourishing, thanks to an increasing global acceptance of HSI technologies in mining & mineralogy, machine vision and life science & diagnostics. The global market has been segmented on the basis of application and region. Based on application, the HSI market is categorized into food & agriculture, military surveillance, environment monitoring and life sciences & medical diagnostics, together with calorimetry, meteorology, mining & mineralogy, machine vision, and process control. The military surveillance (defence) segment contributed the maximum share with 18.6% in 2014 to the overall market; followed by environment testing and mining & mineralogy. Military surveillance is expected to reach $13.87 million by 2020, at a CAGR of 9.7%. However, the fastest-growing application segment is life science & medical diagnostics, which is expected to grow at a CAGR of 13.7 % from 2014 to 2019.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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PROJECT RESULTS

CAT121

Highly integrated, energy-efficient and cost-effective technologies ensure delivery of 5G mobile networks [EAST]

The award-winning EAST project will ensure the realisation and implementation of 5G mobile networks, while delivering such key benefits as: smaller 5G cells; reduced energy and lower operational costs; improved transmitter switching across bands; and massive MIMO (multiple-input, multiple-output) systems.

True, today's 3G (third generation) technologies provide mobile users access to a fully featured internet. However, speeds are somewhat limited when compared to the content that is currently available; and while 4G can technically reach speeds of up to 100 Mbps, the reality is that most of us experience data rates below 50 Mbps. Furthermore, due to infrastructure issues, there have also been some drawbacks with 4G, such as energy inefficiency and high latency.

Fifth generation (5G) networks could change all of that. As the latest generation in cellular mobile communications begin their roll-out, focus is on the benefits these advanced networks promise to deliver, which include: higher data-rate; reduced latency; energy savings; cost reduction; higher system capacity; and massive device connectivity. In addition, as indicated further in this report, a more robust solution which 5G offers is also necessary to handle the enormous growth in mobile devices and data.

More integrated, efficient and cost-effective 5G networks

Before describing the EAST project, it is important to briefly look at two important design considerations. The first is radio frequency (RF), the rate of oscillation of electromagnetic radio waves in the range of 3 kHz to 300 GHz, and which is the frequency band that is used for communications transmission and broadcasting. If 5G is to actually deliver speeds that are up to 1,000 times faster than the current 4G ones, it would need to utilise the spectrum more effectively.

The second consideration has to do with multi-antenna technologies, such as massive MIMO (multiple-input, multiple-output) systems, which are the most likely candidates to significantly improve spectral efficiency in 5G networks. Implementing MIMO with large scale antenna arrays, typically with 64 or more transceiver elements, should increase the capacity of a cell well beyond what is achievable today.

EAST started out by defining several design and architectural elements, which were deemed key to a successful 5G implementation: namely, the creation of smaller cells and the use of MIMO or smart-antenna techniques operating at higher bandwidths with lower power consumption. However, by introducing more (small) cells with multiple transmitters, data handling, integration, power consumption and cost reduction became crucial and needed addressing.

To achieve this, major steps were taken at the system/design level (novel transmitter architectures), at the technology level (new silicon processes and packaging solutions), as well as, in the development of characterisation and modelling tools to handle the increased bandwidths and linearity requirements of 5G network applications.

In particular, the following issues were dealt with accordingly:

- Enhanced data rates (video bandwidths up to and beyond 100MHz);
- Higher transceiver integration (10-100 times size reduction);
- Higher functionality (MIMO/smart antenna);
- Drastic cost-reduction (10-100 times compared to micro/macro base stations);
- Re-configurability (multiple-transmit bands);
- Higher overall system efficiency (greater than 60%);
- Reduced energy consumption;
- Shorter time-to-market.

It should be noted that EAST also focused on the overall integration of RF front-ends for 5G base-station and handset applications with their critical building blocks, namely: the signal up-conversion / conditioning (digital pre-distortion), power amplifiers, low-noise amplifiers, switches and antenna.

PROJECT CONTRIBUTES TO

- Communication
- Energy efficiency
- Digital technology
- Process development
- Manufacturing science

PARTNERS

NXP Netherlands
BESI
Bruco
Anteverta-mw
Nokia
TU-Delft
TU-Eindhoven
TNO

COUNTRIES INVOLVED

- Ireland
- Netherlands

PROJECT LEADER

Dre van den Elshout
NXP Netherlands

KEY PROJECT DATES

1 May 2015 - 30 April 2018

And there are significant benefits. EAST will lead to smaller and more energy-efficient 5G cells and massive MIMO systems in the future. Concepts developed in this project will enable switching 5G transmitters across bands without creating unwanted signals in other bands. They will also reduce power consumption and therefore lower costs for network operators. On the receiver side, the highly efficient antenna concept will allow switching between 5G bands with stronger resulting signals, thus eliminating the need for expensive filter and switching gear. EAST also balances the increase of power consumption with more energy-efficient concepts, as mentioned previously. Importantly, these improvements in power consumption will also decrease the environmental footprint of 5G and drive cost savings for network operators deploying 5G.

Necessary close co-operation and collaboration

The EAST consortium consisted of vertical and horizontal actors – from technology developer and provider to system integrator – who provided all the necessary project competences and resources. Development work in EAST resulted in four patent applications. Project partners were also active in disseminating knowledge gained from EAST, and in promoting the project and its achievements through conference papers and journal contributions (22), and technology workshops (5). In addition, EAST provided research work for several technical-university master's and PhD candidates.

Growth in mobile devices, apps and data will drive 5G

Even though analysts predict that the number of smartphones sold in 2018 will be slightly lower than in 2017 (the industry's first ever annual decline), sales are nevertheless substantial at 1.4 billion units per year. Crucially, mobile devices (smartphones and tablets) will soon be – if they are not already – the preferred platform to access the internet, overtaking the computer In addition, an increase in the number and usage of apps and online services, like mobile payments and video streaming, and future ones (such as controlling 'smart' home appliances), means that mobile data is not only growing in quantity, but also in value to business and consumers. According to Statista, a statistics portal, global mobile data traffic is projected to increase nearly sevenfold between 2016 and 2021. According to 2018 data, the global mobile population amounted to 3.7 billion unique users. As of 2017, mobile devices accounted for 49.7% of web page views worldwide. And Europe has the highest mobile broadband subscription penetration rate, around 78.2%.

All of this will, in turn, drive 5G deployment. Demand for 5G, once it takes off, should be considerable. According to Statista, 5G is expected to hit the market by 2020. By 2021, the number of 5G connections is forecast to reach between 20M and 100M. Some estimates put the figure at 200M. Crucially, spending on 5G mobile infrastructure for that same year is forecast at around US$ 2.3 billion.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

PROJECT RESULTS

CAT406

Improved mammogram screening through high-quality imaging, fewer retakes, lower X-ray dose and greater patient comfort [NEMADE]

The NEMADE project developed a new mammography detector using a multi-tiles wafer-scale CMOS imager for efficient breast-cancer screening and tomosynthesis. In addition to reducing breast-compression discomfort previously experienced by users, this solution also delivers other societal benefits, together with technical and environmental ones.

Some 450,000 women are diagnosed with breast cancer annually In the European Union and more than 100,000 women die from it every year. Regular screening can significantly reduce the risk. However, there is a downside to it: breast compression is very painful and the X-rays used for screening can be harmful. At the time when this project was proposed, X-ray detectors for mammography screening typically used slow and noisy amorphous silicon-based detectors with direct X-ray conversion which has significant lag. While the performance was sufficient for screening (static application, single image), this way of screening had reached its limits for biopsy, and especially when compared to the emerging tomosynthesis with its dynamic application and sequence of images.

And on the business side, Europe was looking to play a significant role in the screening market, which was then dominated by North American and Asian suppliers.

Efficient, reduced-pain and affordable breast-cancer diagnosis

NEMADE's goals were to improve mammography screening by developing a system capable of consistently high image-quality and fewer retakes, at a lower X-ray dose; and with greater patient comfort.

These project goals translated into several technical objectives and deliverables. Significantly, by replacing the amorphous silicon with a CMOS imager (CMOS or complementary metal oxide semiconductor is a technology for constructing integrated circuits), the mammography detector – the key deliverable – achieved the higher speeds needed to meet biopsy and tomosynthesis requirements, while still maintaining a low total X-ray dose. Thanks to several important features – like binning pixels, region-of-interest readout, selectable X-ray saturation dose and real-time dose sensing (all enabled through CMOS technology) – a single detector could produce the best possible images and without needing retakes. Furthermore, the lower CMOS noise-level and the use of structured scintillators (a scintillator is luminescent material which, when struck by an incoming particle, absorbs its energy and then re-emits it in the form of light), which combine high-resolution with high light-output, means that all this can be done at a lower X-ray dose to the patient. Crucially, the use of personalised mammography allows breast-compression to be fine-tuned to the patient's needs, thus minimising associated pain.

To summarise, NEMADE's key achievements/ deliverables include:

- A new mammography detector using newly developed multi-tiles wafer-scale CMOS imagers combined with conventional CsI (Cesium Iodide) indirect conversion. This solution includes innovative features at different levels which provide efficient support for screening and tomosynthesis;
- Improvements to the assembly process with changes in tooling to move to a fully automated assembly and to increase more uniform flatness of the tiled CMOS array;
- Evaluation (also through simulations) of the structured scintillator demonstrating high-quality results based mainly on the modulation transfer function (MTF);
- From semi- to fully-automatic adjustment of image receptor height to balance forces and subsequently improve the image quality (by about 10%) and provide comfort to users undergoing mammography.

There were also other achievements. NEMADE delivered prototypes to a significant number of customers/OEMs, resulting in positive feedback and in several cases to business opportunities. The project also generated six patent applications and 10 publications, and consortium members participated in three international trade shows.

PROJECT CONTRIBUTES TO

- Health and aging society
- Manufacturing science

PARTNERS

Teledyne DALSA
SigmaScreening
Scint-X

COUNTRIES INVOLVED

- The Netherlands
- Sweden

PROJECT LEADER

Jan Bosiers
Teledyne DALSA, Netherlands

KEY PROJECT DATES

January 1, 2015 - December 31, 2017

Environmental and societal benefits

NEMADE delivered personalised and affordable mammography scanning that strongly improves patient comfort, image quality and diagnosis. Crucially, this will lead to fewer complications in breast cancer – and thus a higher degree of safety for the patient – for two reasons. Firstly, better accuracy of screening through vastly improved image-quality means fewer retakes and a lower overall X-ray dose. And secondly, reduced pain caused by breast compression and higher efficiency will reduce health-care costs and also result in a higher percentage of women participating in the screening programmes (fewer no-shows) and with fewer complications.

On the technical side, the scintillator uses silicon-based CMOS/MEMS technologies to etch deep pores in silicon to be filled with a scintillator. Combining this with CMOS imagers results in true silicon photonics. Using silicon as a 'carrier' for the CsI scintillators facilitates environmental protection. In addition, the scintillator imager assembly can be made more robust since both parts are now made on silicon, with the same thermal expansion coefficients. The new environmentally robust assembly technology for conventional scintillators also improves overall detector reliability.

Promising market and market position

Screening programmes that drive overall mammography demand are taking off, especially in emerging markets, where a larger percentage of income is spent on health care as income per capita grows. Notably, this increase in income is also leading to the adoption of a more Western lifestyle, which is causing (for some unknown reason) a higher incidence of breast cancer.

The full ramp up is planned and programmed for mid-2018. Encouragingly, more and more patients and hospitals are requesting this new technology. Based on feedback from 2016, expected business volumes will increase from € 15m in 2019 to some € 25m in 2020. The total addressable market (TAM) for digital mammography will exceed US$155m in 2019, the highest growth-rate among all types of X-ray applications for flat panel detectors.

Meeting a business objective, NEMADE has significantly strengthened Europe's current market position in mammography X-ray systems and detectors, even challenging the dominant position of a key North American competitor.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

PROJECT RESULTS

CAT801 | Promising outlook for advanced packaging products thanks to improved production yield in high volume manufacturing [TSV-Handy]

The TSV-Handy project met its key objectives: the brightfield inspection of heterogeneous 300mm wafers; development of metrology and new logistical concepts for wafers on 380mm frames; and improvements to temporary bonding and debonding processes. Key achievements included innovative frame-handling and a flexible metrology platform equipped with multiple sensors.

Through silicon via (TSV) is a more-than-Moore (MtM) chip technology which improves the density of a device by stacking dices (3D) onto an interposer, or arranging them horizontally side-by-side (2.5D). This technology is also applied to reconstituted epoxy/mould compound wafers with through polymer VIA (TPV) in fan-out wafer-level packaging (FO-WLP) technology, an enhancement of standard wafer-level packages developed to provide a solution for semiconductor devices requiring a higher integration level and a greater number of external contacts. In addition, this technology provides a smaller package footprint with higher input/output (I/O), along with an improved thermal and electrical performance. Consequently, it has become the preferred technology for system design and the focus of attention.

Boosting high-volume TSV manufacturing and improving production yield

TSV-Handy's focus was on supporting a high-volume manufacturing (HVM) ramp-up and on improving the yield for manufacturing advanced packaging products. In particular, it addressed challenges posed by 3D TSV and FO-WLP technologies, and by the increase in substrate types which typically have different mechanical behaviours and physical properties.

Key project activities and resulting benefits were:

- Heterogeneous handling development of 300mm wafers with brightfield inspection (a technology that uses light sources to find defects during the transistor fabrication process in a fab). This resulting innovative way of handling glass and recon will improve European competitiveness because heterogeneous handling is not generally available on the European EFEM market, especially the mid-end part;
- Developing metrology and new logistical concepts for wafers on 380mm frames, which resulted in an innovative frame-handling and a flexible metrology platform with multiple sensors. This should improve the position of European suppliers in a very competitive metrology market where the key players are the USA, Israel and Asia, and where there are only two known European suppliers with frame-handling capabilities, and no frame EFEM suppliers which can service the production area;
- Frame logistics development for HVM, which resulted in a front-opening unified pod (FOUP) frame, shipper and a frame with radio-frequency identification (RFID) prototypes compatible with an automated HVM environment. This should increase the position of European suppliers of products for handling in-process wafers mounted to frames (typically open style cassettes that are multi-piece, custom-fabricated carriers often made of metal which are high-cost, with low particle-control, and part-to-part variation due to low-volume and a custom fabrication technique);
- Improving temporary bonding and debonding processes for the 3D integration market and HVM, resulting in key reproducible processes using novel adhesive materials transferable to major IC makers. This should give European bonding and debonding vendors a competitive edge.

Adopting a modular approach called SMART platform (a common robotics and software core interfaced with several loading stages and end-effectors), this project delivered modular equipment capable of manipulating several types of wafers, without any hardware reconfiguration. In addition, smart software-management was developed to help end-users improve equipment flexibility and up-time.

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Health and aging society
- Digital lifestyle
- Design technology
- Process development
- Manufacturing science
- More than Moore

PARTNERS

RECIF
ENTEGRIS
EV Group
UNITY-SC
AMKOR
STMicroelectronics
CEA LETI
IMEC

COUNTRIES INVOLVED

- France
- Germany
- Austria
- Portugal
- Belgium

PROJECT LEADER

Isabelle Saucourt
RECIF

KEY PROJECT DATES

1 April 2015 - 31 March 2019

In particular, TSV-Handy delivered two equipment front-end modules (EFEMs):

- A platform capable of handling frames, on which a metrology tool with lithium indium diselenide (LISe) and Spiro sensors was adapted, and a load-port designed for a FOUP;
- An atmospheric EFEM to handle silicon and recon wafers with an integrated brightfield inspection module.

Importantly, this project was also able to demonstrate that the heterogeneous inspection and frame metrology equipment could respond to the wafer handling and inspection/ metrology requirements for mid-end manufacturing. In addition, the resulting prototypes were successfully installed and evaluated according to their usage in terms of automation, cleanliness, and stability.

How TSV-Handy will impact business and markets

TSV-Handy could impact business in several ways. Firstly, it could raise productivity levels, but also generate new products. This will drive business and in turn increase employment. It will also promote and maintain high-tech European companies and semiconductor centres.

Crucially, this project also secures competitiveness in several European industry sectors. The FO-WLP packaging market is starting to grow as this new technology platform begins implementation. According to YOLE, a French research institute, in 2016 90% of the FO-WLP market was driven by eWLB, a breakthrough technology which provides a more space-efficient package design, enabling a smaller footprint, and higher density input/ output. Furthermore, since tapes can no longer be used for ultra-thin wafers, new wafer-handling technologies have to be developed, which means that the use of temporary bonding technology is also growing. Along with standard approaches, we now have temporary bonding with reconstituted wafers for FO-WLP.

The production of TSV chips and wafers is forecast to have a significant average continuous growth rate in the coming years (107% throughout 2013-2018), given that industry can address the challenges related to technology and manufacturing cost. By 2016, the temporary bonding tool market-value for TSV and FO-WLP was forecast at US$222m. The TSV Handy project will also help boost and stabilise this position for novel applications targeted in the TSV-Handy project. This is particularly important for Europe, considering the major competition is in Asia and US.

Europe offers more flexible and versatile solutions in metrology inspection over its competitors, given that it is the only solution-provider capable of measuring moulding compounds before thinning (required for advanced-packaging solutions). Furthermore, TSV-Handy is expected to improve equipment to satisfy current and upcoming demands. Potential sales for a key European supplier were put at somewhere between €5m and €10m by 2019.

Finally, new business generated by automated wafer-handling equipment is expected to increase an important European supplier's volume by 30%. Estimated revenue generated from this segment should be at least €5m per year by 2020. Furthermore, for another key European automated shipping-carrier supplier (which already has some 40% of the worldwide market and where Europe represents 20% of its business), project deliverables are expected to generate a worldwide share of 40-60%, with 40% of that business in Europe. In addition, this same supplier also expects more than a 60% market share in in-fab 3D wafer-handling products worldwide, with 30-40% of that business in Europe.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

PROJECT RESULTS

CAT802

European equipment suppliers benefit from smart analysis methods for 3D integration in advanced microsystems and materials

[SAM^3]

The innovative co-labelled EURIPIDES²-CATRENE SAM3 project is gearing up to meet the challenges the next ten years will bring as we witness the next big changes to package materials, highlighting the need for proper characterisation and failure-analysis techniques.

Complex microelectronic devices are at the very core of such innovative projects as the futuristic Smart Cities. This makes More-than-Moore (MtM), System-in-Package (SiP) and 3D high-density integration essential in the design of these projects. To ensure that these devices remain at the technological cutting-edge, we are already witnessing new developments in package materials and processes. This, in turn, will require effective analysis techniques to understand new failure modes and reliability-limiting factors caused by thermo-mechanical mismatch, residual stresses and interaction of new materials and processes.

Now, at the time of this project, there were challenges to be dealt with. For instance, failure-analysis techniques to localise electrical defects in SiP devices with multilevel wiring and efficient and artefact-free sample preparations for physical analysis techniques were limited. This led to a strong interest in '3D-SiP' integration and MtM performance, together with miniaturisation and cost-reduction. Notably, failure analysis was first recognised as a major enabler. This, in turn, called for the development and qualification of new diagnostic tools and advanced methods for material characterisation, defect localisation, sample preparation and physical-failure analysis.

Driving competiveness through quality, price and failure diagnostics

The prime objectives behind the SAM3 project were to strengthen global competitiveness of European Union semiconductor and system suppliers in designing and manufacturing reliable, high-quality and cost-effective MtM and SiP products, and to foster a closer cooperation with suppliers of failure-diagnostics tools in order to shorten product-development cycle times.

This project also aimed at strengthening global competitiveness of innovative diagnostic-tool suppliers by providing them access to the latest available MtM and SiP technology developments. Crucially, implementing innovative failure-localisation and analysis methods and tools in MtM and SiP developments would secure reliability and reduce field returns. Furthermore, by supporting suppliers of semiconductors, systems and diagnostic equipment, research institutes could establish an international, competitive infrastructure and know-how.

The SAM3 project was run by a consortium from France and Germany, comprising four leading European semiconductor and system suppliers, ten tool providers and four research institutes, which provided specialist expertise and experience in such areas as failure localisation, preparation and analysis, and material characterisation.

Project activities – mainly focusing on the impact of analytical methods and the causes of reliability failures – can be summarised as follows:

1. Early technology concept phase:
   - Assess new failure mechanisms, physics of failure;
   - Design for reliability and virtual prototyping (finite element simulation).
2. Technology & assembly-process development:
   - Mature interconnect technology;
   - Robust production processes;
   - Efficient material sets.
3. Product development & qualification:
   - R&D to get first qualified products shipped to the customer.
4. Manufacturing:
   - R&D to improve quality & yield;
   - Inline-check, sampling, monitoring.
5. Customer returns, field failures.

Significant progress was made in failure localisation, preparation and analytical characterisation in 3D packages and SiP. In particular:

- Electrical characterisation and failure narrowing;
- Package-level non-destructive defect localisation;
- Device opening and target preparation;
- Chip-level defect localisation;
- Defect physical analysis;
- Determining root causes of failure;
- Development of failure analysis flows.

Additional significant results with respect to failure analysis equipment were:

- A novel concept for defect localisation by scanning acoustic microscopy (SAM) with GHz-SAM, for example pad cratering;
- Enhanced lock-in thermography (LIT) systems for improved hotspot localisation and thermal mapping;
- A prototype for nanoprober and EBAC (electron beam absorbed current) systems;
- A preparation flow for combined laser/plasma-

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Safety and security
- Energy efficiency
- Sensors and actuators
- Process development
- More than Moore

PARTNERS

Infineon Technologies AG / Robert Bosch GmbH / MUEGGE GmbH / PVA TePla Analytical Systems GmbH / Point Electronic GmbH / SmarAct GmbH / WITec GmbH / 3D-Micromac AG / STMicroelectronics (Grenoble2) SAS / STMicroelectronics (Rousset) SAS / STMicroelectronics (Tours) SAS / Thales Systèmes Aéroportés / Thales Research and Technology / Digit Concept / Orsay Physics / Predictive Image / Sector Technologies SAS / CNRS (represented by LP3-Marseille, LEPMI-Grenoble, and GREMAN-Tours) / GREMAN Tours University / Fraunhofer IMWS / Reutlingen University

COUNTRIES INVOLVED

France
Germany

PROJECT LEADER

Klaus Pressel
Infineon Technologies AG

KEY PROJECT DATES

1 October 2015 - 31 December 2018

FIB (focused ion beam) for fast and precise SiP cross-sectioning;

- In-situ delayering by plasma FIB;
- A tool concept for plasma etching of wide bandgap materials;
- New methods for quantitative dopant characterisation;
- A new method for modelling acoustic beam behaviour in microelectronic components tested.

Commercial potential and early market introduction

Importantly, collaborative work by the project's major semiconductor and system suppliers, together with the failure analysis of compact SiP solutions by equipment and method suppliers, produced results with high commercial potential. Here are some notable examples:

- Novel plasma etching tool: achieves an etching rate of better than 1 µm/min for silicon carbide (SiC) by combining a microwave-driven remote plasma source driven by radio-frequency (RF) ion etching;
- Extended optical residual stress measurement: allows maximum efficiency for residual stress measurements on Si devices based on a new spectrometer design extending the frequency range from visible to near ultraviolet (UV);
- Scanning acoustic microscopy µ-crack detection: enables defect analysis on stressed bond-pads, flip-chip contacts and copper-to-copper (Cu-Cu) bonds using SAM in the GHz frequency domain;
- New current imaging system for scanning electron microscopy (SEM): including new electronics and software for resistive defect localisation, which allows parallel probing and highly sensitive EBAC/RCI analysis, as well as in-situ needle-cleaning process to increase throughput;
- Novel 8x SEM in-situ nanoprober system: used for IC-level diagnostics, based on closed-loop piezo technology for large scale positioning with nm precision;
- Improved high-precision, ultra-short-pulse laser system: enables fast cross-sectioning preparation of complex SiP components by combined laser/FIB workflows. In addition, conformal backside thinning of dies (a technique to produce ultrathin dies) is now possible;
- Plasma-laser sample preparation: applies 2.45 GHz cold plasma allows the removal of epoxy moulding compound; and a 512 nm pulse-shaping laser reduces the cross-section effort before FIB significantly – from hours to minutes;
- Faster in-situ plasma FIB: used for delayering and combined laser-/plasma FIB cross-sectioning to enhance preparation throughput;
- Development of reference samples for acoustic microscopy: allows qualification of SAM analysis tools by using test samples with defined artificial defects. Samples are stable over time and easy to use;
- Novel thermography system: multi-point acquisition of thermal transient events and temperature measurements (accuracy to 1°C) on die and complex packages;
- Improved EOTPR system: enables short and open localisation on complex packages with an accuracy of 5 µm.

SiP integration is widespread

Thanks to miniaturisation, SiP has become an enabler for heterogeneous integration. The SiP market is growing and 3D-SiP solutions are appearing in products and components in various sectors: such as automotive electronics (3D image sensor chips); energy generation and energy distribution (like Smart Grid); industrial electronics, where SiP growth of over 20% is predicted; and in such sectors as solid-state lighting, medical and aeronautics.

All this is backed by market statistics. Yole's 2019 report predicts a CAGR of about 11% between 2018 and 2023 for the total assembly market for RF-SiP components in mobile phones. In their market report from May 2019, Zion Market Research forecast a CAGR for SiP of around 8.1% between 2019 and 2025. And market growth is supported by statistics from Allied Market Research, which expect the global SiP packaging technology market to reach US$30 billion by 2022, growing at a CAGR of 9.0% during the forecast period 2016–2022.

Crucially, SAM3 secures European competitive power in key industry sectors already mentioned, allowing Europe to hold a strong position in high-density, complex SiP technologies. All this is occurring just as mass production of some microelectronic devices moves out of Europe. This makes it even more critical for Europe to develop intellectual property in this emerging field to maintain existing employment levels, develop replacement products and reap financial benefits.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

CATRENE (E! 4140), the EUREKA Cluster for Application and Technology Research in Europe on NanoElectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

PROJECT RESULTS

CAT209

Robust and user-centric technology platform for secure wearable objects aimed at Internet of Things and Smart City applications

[H2O - Human to Objects]

H2O creates a technology platform for the development and customisable integration of secure wearable objects. It delivers solutions which are cost-effective, ensures privacy and security, as well as enables easy and user-friendly interactions. The project also validates the platform's capabilities with the help of representative use cases.

Businesses, military forces and medical professionals have been using wearable technology for decades, but the private consumer market has only recently started to feature items, such as smart glasses, smart watches, hearables, fitness and health trackers, smart jewellery or smart clothing. The most successful wearable devices on the market right now are smart watches and health and fitness trackers.

However, with the market growth for wearables also grew calls to simplify the user-interface and to make customisation much easier. Furthermore, lack of proper security and privacy protection were a constant cause for alarm. Hence, the underlying rationale for the H2O project was to give wearable computing and the target business areas – Internet of Things (IoT) and Smart-City applications (notably e-Mobility, e-Health and e-Commerce) – a real boost by providing the missing key elements required to further drive these businesses, while continuing to improve the digital lifestyle of the user.

Towards a secure and user-friendly wearables platform

The H2O project defined, designed, developed and validated a technology that establishes secure, bidirectional wireless interaction between objects or individuals, based on capacitive conductivity of human skin. In addition, the project investigated human-to-object interaction in different application areas, and also manufactured H2O-specific devices and integrated them in the use-case-specific architecture deployed in six demonstrators.

The project's main objectives were to:

- Provide a robust, open, technology platform (hardware, embedded software and management tools) for the development and customisable integration of a large variety of secure wearable objects aimed at providing user interaction which is trusted, privacy-preserving and easy to establish in future IoT and Smart City environments;
- Address the double challenge of high security in an open and a non-secure environment supporting multi-tenants business models;
- Provide cost-effective and fast operational solutions;
- Validate the capabilities of the platform in representative IoT or Smart-City use cases, such as eHealth, e-Mobility or e-Commerce. The validation process included several facets, such as user panelization, fast-track prototyping, living labs and pre-deployment schemes in real working conditions.

The main project deliverables were:

- A high-performance, reliable, ultra-low-power body communication coupling (BCC) technology;
- A representative set of non-intrusive, secure, low-cost, wearable devices, suitable for several application domains pertaining to IoT or Smart-City. Robust and easy-to-use form factors (such as watch, bracelet and clips) suitable for target applications were also implemented;
- A fully trusted and privacy-protecting transaction environment, enabling objects which users wear or touch to seamlessly initiate applications or communicate with other objects;
- An open software-development kit (SDK) and application-certification tool-chains which facilitate third-party development of wearable computing apps, and ensure such apps can be automatically verified before being remotely loaded onto user-owned wearable devices;
- A complete reference and trusted-security architecture enabling seamless, secure synchronisation of wearable devices. This synchronisation includes loading credentials onto a blank wearable device;

PROJECT CONTRIBUTES TO

- Communication
- Health and aging society
- Safety and security
- Digital lifestyle
- More than Moore

PARTNERS

Gemalto
CEA LETI
CEA LIST
Worldline
IDEMIA
Insight SiP
STMicroelectronics
Astus
Trusted Labs
IDATE
Johnson Controls International
IPCB
IT Aveiro
Beyond Vision
IMA
Tyndall

COUNTRIES INVOLVED

- France
- Ireland
- Portugal
- Czech Republic

PROJECT LEADER

Christian Dietrich
Gemalto

KEY PROJECT DATES

01 January 2015 - 31 November 2018

- A pilot implementation of wearable-computing scenarios in IoT or Smart-City application domains, together with initial quality-of-service (QoS) or quality-of-experience (QoE) feedback.

Spreading the good news

H2O continued the standardisation effort (started in a previous project) to promote the replacement of the secure element (SE) legacy framework set up in the early 1990's, which allows for the separation of hardware and software elements and also deals with other key issues such as privacy. This new standardisation framework will ease the deployment and implementation of security functions in the core of the chips integrated in the upcoming devices.

H2O's creative work resulted in eight patent applications and more than seven articles, reports and papers, which were presented at conferences or submitted for publication (and some even won awards). Project members participated in some 50 events, such as workshops, conferences and exhibitions, all of which supported the dissemination of the knowledge and experience gained from the project, while promoting and marketing its achievements and products.

Targeting premium secure-wearables markets

According to Gartner, a research company, worldwide wearable device sales will grow 26% in 2019 and worldwide shipments will reach 225m in the same year (an increase of 25.8% from 2018), growing to 453m units by 2020. Notably, the total addressable market for H20, when considering only the selected use cases analysed in the project, is between five and 10 million devices (a small share of the wearable market), with a large part coming from access control and payment. However, the market for pure payment or omnichannel (the seamless multichannel approach to selling regardless of shopping method) access control will be more difficult to target, due to increased competition from mainstream wearable stakeholders integrating payment schemes, and a price war in the consumer market.

Indeed, if the overall volume is expected to be small, the overall value could be significant, at up to €3 billion of the total available European market. H20 will position its products in the premium secure-wearable markets, thanks to its notably differentiating features (over those in traditional wearables), namely its focus on advanced seamless security/privacy, something most end-consumers are not ready to pay for, and not nearly enough aware of. As a consequence, the 'sweet spots' are logically in business-to-business (B2B) markets, which can not only value these features, but also adopt the relevant processes needed to implement them. The top market is therefore access control for various vertical sectors: corporate, industry, banks and the like. Here, H20 products can differentiate themselves from others, thanks to such additional features as: ultra-wideband (UWB) for indoor localisation/tracking; tight security based on eSE and BCC; medical sensors for healthcare; near-field communication (NFC) for payments; in addition to data storage and logical security. A prime target for H20 products could therefore be high-end markets for access control and healthcare.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

PROJECT RESULTS

CAT601

A coherent Chip-Package-Board/System Co-design environment reduces costs and improves time to market, design reliability and performance [SiPoB-3D]

What compact system-integration needed to reduce costs and mitigate the risk of failure was an effective design environment with the facility to design over all three domains chip, package, and board/system. This allows extensive pre-fabrication testing and changes before compact electronic systems are finally released for manufacturing. That is exactly what the Co-design for System-in-Package-on-Board (SiPoB-3D) project delivered.

For reasons of performance, size and cost, technologies like More Moore (MM), More than Moore (MtM), three-dimensional high-density 3D IC, system-in-package (SiP), as well as passive integration are combined. Compact system-integration, as this process is called, also involves a variety of different materials. However, because of inherent complexities, this process is expensive and risk of failure high. It also raises challenges with the interface between packaged chip and board (PCB). Ideally, what is needed is a user-friendly, coherent Chip-Package-Board/System Co-design in which designs can undergo extensive pre-fabrication testing and changes – but without the associated costs – before they are finally released for manufacturing.

Coherent and effective cross-domain design environment

SiPoB-3D largely aimed at addressing seven key challenges which were considered major issues:

1. Need for a coherent design environment: chip, package, and board/system.
2. Need for improved data exchange and design interfaces
3. Alignment of different tool landscape for Chip-Package-Board/System Co-design
4. Handling a variety of technologies (at Chip-Package-Board/System Co-design level);
5. Avoiding expensive hardware prototypes;
6. Dealing with thermal management across domains;
7. Supporting proper material selection, especially in respect to mm-wave parameters and Coefficient of Thermal Expansion (CTEs).

To handle these and other issues, a well-balanced project consortium was appointed, bringing together the experience and expertise of semiconductor suppliers, major suppliers with strong board capabilities and applications which could be applied to better understand the requirements and related problems and solutions in connecting the three domains. In addition, project research and support were provided by several European academic institutions.

Excellent project results have been achieved. SiPoB-3D delivered the prerequisites for such a design environment, which supports development within a single company as well as jointly between companies. The environment also reflects a coherent consideration of chip, package, and board/system, critical for future semiconductor product-development. There are obvious future benefits. New innovative multi-chip SiP and 3D products, new applications, and larger application windows are expected from such a coherent design environment and new methodologies. In addition, new products from tool suppliers are expected and board suppliers can significantly improve their data management, as well as, benefit for technology improvements (like higher line/space density or chip embedding).

Crucially, the project itself generated several success stories. It investigated the design environment and applied it to different types of systems containing both complex logic and analogue devices. Furthermore, the project's device manufacturers developed and improved the methodology and implemented its design capabilities into their internal tool environment for right-first-time design. Now these companies can develop and optimise complete SiP devices (together with their customers) faster, better, and more economically.

There were other notable project activities and deliverables, such as assembly design kits for many relevant package technologies, including lead-frame packages and complex laminate ones. This is an essential base to optimise designs over all three domains of chip, package, and board/system. In addition, one of the project's semiconductor suppliers deployed an optimised SiP and the 3D design-flow suite within its entire design team, working with technology nodes in non-volatile memory or CMOS. This reduced the cycle time for complex 3D/SiP system-on-chip (SoC) designs by around 20%, and minimised the risk of re-spins by integrating low power and board-level checks for SiP/3D designs. In addition, this design environment is being used for very advanced nodes below 28nm. A flip-chip checker, which enables both substrate

PROJECT CONTRIBUTES TO

- Automotive and transport
- Digital technology
- More than Moore
- More Moore

PARTNERS

Infineon Technologies AG
Continental Automotive GmbH
Computer Simulation Technology GmbH
Hitex Tools Development GmbH
Schoeller Electronics Systems GmbH
Symeo GmbH
STMicroelectronics SA
STMicroelectronics (Grenoble 2) SAS
Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e. V. (FhG)
with its institutes EAS/IIS and IZM ASSID
FAU Erlangen-Nuremberg
CEA-LETI
Université de Savoie IMEP- LAHC, Chambéry, Le Bourget du Lac

COUNTRIES INVOLVED

- Germany
- France

PROJECT LEADER

Klaus Pressel
Infineon Technologies AG

KEY PROJECT DATES

01 March 2016 - 31 May 2019

and silicon designers to quickly validate the bump matrix and assembly rules, is fully integrated in the company's co-design framework environment, from front end to back end manufacturing.

Furthermore, simulation and modelling of electrical and thermal performance of integrated antennas were implemented in a mm-wave SiP toolbox. Special focus was on determining material parameters and their characterisation by innovative methods up to 100 GHz. Significantly, these results pave the way for the design of mm-wave products of much larger complexity, and for improving systems in terms of resolution, production cost and size.

Finally, project results are already being applied to design 5G and mm-wave applications (like 77 GHz radar or advanced logic in microcontrollers). The project will also open new market segments for mm-wave radar systems, like collision avoidance and smart agriculture as well as expanding suppliers' modelling and simulation portfolios, from electro-magnetic and thermal performance, to thermo-mechanical.

Significant collaboration and information sharing

Key to the success of SiPoB-3D was, on the one hand, the involvement of project experts on the chip, package and board/system level; and on the other hand, the verification in hardware. Information sharing was also excellent. The project consortium distributed some 80 reports and provided more than 30 presentations, including one at Cadence Forum 2019 where it received an award for the best presentation.

Impacting design environment, science and education

SiPoB-3D design environment ("backbone") has been introduced by semiconductor partners for already 80% of their complex devices. More than 60 design engineers of the involved chip suppliers are already actively using the backbone design environment for their Chip-Package and Board (PCB)/System co-layout tasks.

SiPoB-3D also impacted science and education: several Bachelor of Science, Master of Science, doctoral and post-doctoral students participated actively in the project as part of their education and related projects.

A promising SiP market

One focus of SiPoB-3D was on SiP applications, which increasingly affect the electronics market. Due to miniaturisation, SiP has become an enabler for heterogeneous integration, and the SiP market is growing, with 3D-SiP solutions appearing in products and components in various market sectors such as automotive electronics (3D image sensor chips), energy generation and energy distribution (Smart Grid), industrial electronics, where SiP growth of over 20% is predicted and in such sectors as solid-state lighting, medical and aeronautics.

All of this is reflected in market-statistics publications; Yole's 2019 report predicts a CAGR of about 11% during 2018-2023 for the total assembly market for RF-SiP components in mobile phones. In their market report from May 2019, Zion Market Research forecasts a CAGR for SiP of around 8.1% during 2019-2025. Growth is also supported by statistics from Allied Market Research, which expect the global SiP packaging-technology market to reach US$30 billion by 2022, growing at a CAGR of 9.0% during 2016–2022.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

CALL 8

PROJECT RESULTS

CAT311

Consumer electronics' upgrade speeds up implementation of innovative automotive electronics and cuts costs through mass production [TRACE]

The Technology Readiness for Consumer Electronics (TRACE) project developed a design methodology and associated processes to help convert, qualify and release low-cost, mass-produced consumer-electronics components for automotive purposes. It also created demonstrators for highly-automated driving and autonomous infrastructure interaction. Crucially, future products are already being designed, aiming at faster development with lower costs and improved properties.

Semiconductor components provide practically all new functions needed in the automotive and industrial-automation industries, such as highly automated driving, connected vehicles, advanced driver-assistance systems, but also co-operative production and human-machine interfaces. However, the semiconductor market is largely driven by the consumer-electronics (CE) sector, which offers opportunities for much higher volumes than the automotive electronics (AE) or industrial automation ones, and thus offering higher and faster returns of investments.

So, what is the way around this problem?

Upgrade methodology and tools for automotive electronics

A logical response is to 'upgrade' the semiconductor processes and underlying technologies, not often qualified for use in automotive. With that in mind, TRACE's key objective was to develop semiconductor manufacturing processes and tools that would cut costs and speed up implementation of innovative electronics in the automotive industry. It sought to break new ground by adapting low-cost, mass-production techniques used to produce semiconductor components for CE devices to the high safety and reliability standards required for vehicles.

Besides activities on semiconductor process, component and package level additional measures were investigated and established on system hardware, software, and testing and qualification level. This allows to mitigate risks and identify effort- and cost-optimized solutions along the complete supply chain.

To this end, a design methodology (the TRACE methodology) and associated processes were developed to upgrade, qualify and release low-cost, mass-produced CE components for use in automotive. This complete, methodical framework optimises the design of the electronic control unit (ECU) – which incorporates CE semiconductor components – in order to enhance its capabilities to a level needed in individual automotive applications. The corresponding design-flow was also implemented using a database-supported toolset. In addition, knowledge gained from demonstrator optimisation was deployed to identify general, strategic and long-term areas of action. TRACE initiated a global network, along the electronics supply chain. Contacts with many different committees were established with a spectrum from lobbying and networking (e.g. within IPC, ECPE, AEC, EPOSS, SEMI, ...) to contributions to standards and best practice (e.g. within IEEE, JEDEC, ZVEI, ...). TRACE initiated an expert group within VDE-ITG (MN 5.7 "Platform for automotive semiconductor requirements along the supply chain") with the target of standardization of the TRACE methodology and its sustainable global establishment. The Global Automotive Advisory Council of SEMI sponsors the initiative, thus bringing it to international level.

In addition to the development of guidelines for CE technology readiness, the TRACE methodology also contains approaches to lifecycle aspects of products and systems. The results of the lifecycle-analysis guide (a starting point for further research in this area) showed that data transparency in this domain is limited. Preliminary results also show that the use of a rare resource (like e.g. tantalum) immediately leads to higher environmental impacts.

Central to this project was the use of CE components in a safety-critical environment. It was shown that test methods used to ensure the functionality of CE electronics in safety-relevant systems had to be adapted according to system requirements. Unavailability or late availability of tested components can hinder developing safety-relevant functions. TRACE worked on test methods that helped to circumvent this situation. Components can be tested within a system-like setup during development, thus improving test coverage, and allowing to lower the overall effort. This, in turn, should have a significant impact on the overall development time.

Several demonstrators for highly-automated driving and autonomous infrastructure interaction were developed, and the functionality of systems using components adapted for AE demonstrated were tested and validated. The Detection and Ranging Demonstrator focused on the car implementation and first-test drives. The Navigation Demonstrator compared the results of CE components with an

PROJECT CONTRIBUTES TO

- Communication
- Automotive and transport
- Health and aging society
- Safety and security
- Energy efficiency
- Digital lifestyle
- Digital technology
- Sensors and actuators
- Process development
- More than Moore

PARTNERS

Robert Bosch GmbH (CO) / AKKA Technologies / ams AG / Berliner Nanotest and Design GmbH / BMW AG / Catena / CEA / Chemnitzer Werkstoffmechanik GmbH / Continental / Coventor / Daimler AG / Delft University of Technology / FH Johanneum / Fraunhofer-Gesellschaft / FRT GmbH /Goepel electronic GmbH / Heliox / iMAR Navigation GmbH / Imsys AB / KTH Royal Institute of Technology / Nexperia Germany GmbH / NXP Semiconductors Germany GmbH / NXP Semiconductors Netherlands BV / QRTech / Rise IVF AB (formerly Swerea IVF AB) / Siemens AG / Smile (formerly Open Wide) / STMicroelectronics Grand Ouest / STMicroelectronics Grenoble / STMicroelectronics SA / Tronic's Microsystems (TDK Tronics) / TWT GmbH Science & Innovation / Université Bordeaux / University Bremen / University Siegen / VEDECOM / Volkswagen AG / Volvo Car Corporation

COUNTRIES INVOLVED

- Germany
- Austria
- France
- Netherlands
- Sweden

PROJECT LEADER

Andreas Krauss
Robert Bosch GmbH

KEY PROJECT DATES

11 April 2016 - 10 October 2019

AE reference system. Several concepts for improvement of performance and risk mitigation were successfully demonstrated. Both demonstrators were tested in lab but, importantly, also on public roads with different driving manoeuvres. A key part of the Intelligent Infrastructure Demonstrator was the design of a sensory system for the surroundings. A capacitive sensor skin was geometrically and electrically adapted to a robot system, measures for risk mitigation were implemented and intensive testing followed. Finally, the Security Demonstrator focused on the security-relevant automotive-communication application in future C2X and C2C communication systems. Test and validation procedures were jointly used to verify this application's security credentials.

Notably, several project partners are already using the TRACE methodology and associated processes to develop future serial products, which are expected to benefit from a faster development time, lower costs and improved inherent properties.

Societal and environmental issues

Innovations – such as advanced infotainment and navigation systems, internet connectivity, vehicle-to-vehicle and vehicle-to infrastructure communications and advanced driver-assistance systems – offer multiple benefits. They can help improve traffic flow and reduce congestion through the use of sensors and communications that allow for cooperative driving and predictive traffic-management. This will not only help optimise the use of available road capacity; but it will also improve the quality of life and the environment.

In addition, intelligent traffic-systems will provide integral system solutions towards road-use and energy efficiency, as well as, road safety. Furthermore, with the introduction of electronic systems for safe and autonomous driving, passive safety-measures will be replaced by active ones, resulting in reduced weights of cars and therefore lower fuel consumption and CO2 emissions. And sensors, such as radar- cameras and the like, will create a safety bubble around the car and reduce traffic incidents.

Driving the automotive industry

Besides covering the necessary modifications and adaptations, the TRACE methodology identified ways to verify that the resulting components, technologies and integrated systems are fully safe and reliable for automotive use. Supporting innovation in the European automotive industry, TRACE brings together the entire value chain – technology provider, semiconductor manufacturers, system integrators, major automotive companies, SMEs and research partners.

The project's business goals are to:

- Allow ground-breaking automotive applications to be developed without the need for automotive-grade components;
- Reduce the time required for innovative system-integration in automotive applications by roughly three years;
- Reduce the cost and time to develop qualified semiconductor components by up to 50%, compared to today's dedicated automotive semiconductor development cycles.

These innovations are also crucial to the continued competitiveness and growth of the European automotive industry, which grew by 8% CAGR in the first quarter of 2017, represents 11% of European manufacturing jobs and exported 6 million motor vehicles equivalent to a 84 billion € trade surplus in 2018, according to ACEA (European Automobile Manufacturers Association) figures. Furthermore, MarketWatch reported in September 2019 that the automotive electronics market is expected to reach 490 billion US$ by 2026. Significantly, innovations in vehicle architectures and systems enable a high-end driving experience, that will sustain automotive-electronics market growth, as well as manufacturing and use of electric vehicles (EVs) in China, North America, and Europe.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

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CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.

PROJECT RESULTS

CAT408

Integrated mobile health monitoring and implantable sensor systems focus on quality of life for the elderly and lowering costs

[NexGen]

The Next Generation of Body Monitoring project (also referred to as NexGen) successfully deployed sensor-based technologies to address health and healthcare issues, and to ease the growing burden of treating a sick and ageing population while delivering other significant benefits.

To help better understand the Next Generation of Body Monitoring (NexGen) project – its objectives, activities and achievements – it is important to first review the situation at the start of this project, some three years ago. There were concerns with ageing, and an urgent need for a healthy, active lifestyle (especially since over 60% of the population were showing early signs of metabolic syndrome) in order to bear the increased pension and healthcare costs. Mobile healthcare systems, based on a multitude of different networked sensors (which enable ubiquitous body monitoring), were seen as an important response to chronic diseases, especially multimorbidity (the presence of two or more chronic medical conditions in an individual). They also looked like the answer to improving the quality of medical services and increasing the independence of the elderly. It was also anticipated that new mass-markets would undoubtedly emerge and nanoelectronic-based components become available in securing reasonably-priced mobile medical-solutions.

However, there were certain missing elements, such as sensors and energy harvesters, standardised protocols and security blocks, as well as, integration technologies for biocompatible and implantable solutions, and cloud offerings for the private and professional sectors. These, together with economic risk, market fragmentation and limitations of then-available micro and nanoelectronic technologies, would limit the benefits of eHealth and hinder a swift and successful commercial launch. The big question then was: what can be done to mitigate some of these barriers and obstacles?

Mobile health-monitoring with implantable and wearable sensors

NexGen focused on the development of integrated, sensor-based systems for mobile health-monitoring applications and implantable sensor systems, offering new highly innovative solutions to improve the quality of life, support, especially, an ageing society and reduce healthcare costs.

The goal was to develop key micro-electronic technologies and components for mobile and wearable healthcare-systems, to be used as a platform for a broad spectrum of applications. This included a set of sensors for body monitoring, improved energy-management systems, enhanced communication and biocompatible integration technologies.

The platform developed covers the two hemispheres of clinical and home-health, and fitness devices in practical use for an ageing population suffering from metabolic syndrome. In this context, reference architectures were defined in order to enable system development (from devices to complete mobile medical solutions) and to enable clinical assessment (including medical approval through the cooperation of healthcare providers and hospitals).

For the glucose monitor, a first proof-of-concept was achieved in a lab. Those results created the basis for the project's technical partners to design a dedicated and highly integrated chip for demonstration and testing (including tests on living animals), ensuring the biocompatibility of the demonstrators. The results of these animal tests not only validated the outcome of lab tests, but also the underlying technical and technology approach.

The results of the multi-parameter supply-chain are also most promising. The various sensors were developed to a 'testable state' and some of them were integrated into an innovative printable patch. Positive results from lab tests enabled subsequent tests, on humans in a hospital environment, to be conducted and with good results. In addition to their supply-chain activities, some project partners also worked on firmware as well as a future cloud offering.

The overall conclusion is that NexGen achieved very good results in developing the necessary innovations for the healthcare sector and generating essential knowledge to support future developments. Furthermore, this project has already seen some of its work being successfully implemented commercially.

Demand for glucose monitoring

There are promising markets in which deliverables from NexGen can be exploited. Diabetes is a key area. The International Diabetes Federation (IDF) estimates that in 2015 approximately 415m people had diabetes worldwide, and that by 2040, this will increase to 642m.

PROJECT CONTRIBUTES TO

- Communication
- Health and ageing society
- Digital lifestyle
- Sensors and actuators

PARTNERS

Infineon Technologies AG
Siemens AG
Senetics health care group GmbH & Co. KG
Infineon Technologies Dresden GmbH
B Braun Melsungen AG
eesy-innovation
NXP Semiconductors Netherlands BV
Philips
Evalan BV
Maastricht Instruments BV
NXP Semiconductors Belgium NV
Quad Industries
SIOEN Industries NV
Stichting IMEC Nederland
IHP GmbH
Charité – Universitätsmedizin Berlin

COUNTRIES INVOLVED

Germany
Netherlands
Belgium

PROJECT LEADER

Tanja Seiderer
Infineon Technologies AG

www.nexgen-monitor.com

KEY PROJECT DATES

01 May 2016 to 30 June 2019

An essential part of diabetes management is the testing of blood-glucose levels, which can be carried out in two ways, through:

1. Continuous glucose monitoring systems (CGMS): are devices that determine blood-glucose concentration continuously and over a longer period of time (for example, 30 days). Here, the glucose concentration in the interstitial fluid is measured and used to calculate the concentration in the blood;
2. 2. Self-monitoring of blood glucose (SMBG): refers to the second monitoring approach, where a drop of blood from the finger or ear is used for the measurement. Users must perform their own measurements at regular time-intervals, using SMBG devices. These devices are cheaper and easier to gain approval from health authorities.

The market launch of CGMS is an important breakthrough in diabetic blood-glucose monitoring. Users who suffer from high fluctuations in blood-glucose levels and who need to measure frequently benefit greatly from this new technology. The global CGMS market was valued at US$878m in 2016 and is expected to reach US$13,672m by 2025. The global SMBG market was valued at US$12,481m in 2016 and is expected to reach US$20,563m by 2025. Importantly, these are areas in which NexGen's glucose monitors can compete.

Smart healthcare and wearables

There are other potential markets for NexGen's deliverables, like the multi-parameter supply chain. The rise in the ageing population, especially in developed countries, has resulted in an increase in chronic diseases and a demand for live and effective monitoring of health conditions. The growing application of internet of things (IoT) in healthcare is one of the key trends that will further stimulate smart-healthcare growth. IoT applications, such as mHealth, provide facilities like medication reminders, remote diagnostics and telemedicine services. Telecom companies are playing a crucial role in the mHealth domain by delivering connected solutions. The smart-healthcare-market forecast report predicts that, fuelled by these factors, the market is projected to grow at a compound annual growth rate (CAGR) of over 24% during the forecast period.

Finally, market developments are also being driven by healthcare professionals interested in equipping their patients with wearables. Many of these initiatives are starting to move out of pilot testing into mainstream care. A good example is the use of a fitness tracker in the weeks before surgery, to reduce the recovery period by ensuring the patient is in a good physical condition.

CATRENE Office
44 rue Cambronne
F-75015 Paris - France
Tel. +33 1 40 64 45 60
Fax +33 1 40 64 45 89
Email catrene@catrene.org
www.catrene.org

www.catrene.org