PROJECT PROFILE

T101: Technology-driven design and test for system innovation on silicon (TECHNODAT)

ADVANCED IC DESIGN AND MANUFACTURING PROCESSES

Partners:

CISC
Dolphin Integration
Fraunhofer Institute
Hirex
Infineon
IROC
ISD
Philips
Simplex
STMicroelectronics
TIMA/INPG
University of Delft

Project leader:

Philippe Garcin,
STMicroelectronics

Key project dates:

Start: January 2001
End: December 2004

Countries involved:

Austria
France
Germany
Greece
Italy
The Netherlands

From one technology generation to the next, each circuit contains more and more devices and each device becomes more fragile. If European chip manufacturers do not continually raise their design and test capabilities, new physical constraints will deeply impair the global quality of emerging system-on-chip technology. The objective of the MEDEA+ T101 TECHNODAT project is to pool the partners' knowledge and expertise to build up powerful and user-friendly design environments. Providing solid design foundations and low-cost testing techniques will simultaneously boost the European semiconductor industry and stimulate a set of leading edge computer-aided design and engineering companies.

Basic cell and memory structures are highly technology dependent. The challenge is to invest in environments that will automatically build and validate blocks, without being limited to a given technology.

There is a permanent need to accelerate and secure the design of logic cells. Demands on computer-aided design (CAD) tools are increased by the need for more data per cell, larger cells and more types of cells – instead of only low-power and fast cells, customers are demanding subtle trade-offs, which increase the number of cell types markedly.

Special attention has to be paid to memory as it occupies an increasing part in future system-on-silicon designs. ROM and RAM require new features such as self-test or self-repair. Non-volatile memory needs an original design flow that did not exist when the project started.

The first goal of the MEDEA+ T101 TECHNODAT project is to develop tools for automatic generation of data for basic libraries and embedded memory blocks, together with automatic validation possibilities taking into account the constraints of new technology generations.

Reducing cost of quality

Another important topic is low cost component testing. The amount of data to be checked is increasing, leading to longer test times, but product life cycles are decreasing, demanding shorter and cheaper test methods. The second important goal of TECHNODAT is to guarantee that the design is good, the resulting chip works properly, and it stays operational in the field.

To decrease test time – and consequently use of test equipment – the project addresses pre-silicon test programme debug by virtual test engineering (VTE) for digital and mixed analogue/digital circuits. System-on-chip (SoC) designs require reuse of tests for intellectual property (IP) blocks for an acceptable test programme development time.

These IP blocks have to come with complete design-for-test (DFT) circuitry and test patterns that rely heavily on standards. Built-in self test (BIST) is important, with developments including test algorithms for both digital and analogue circuits. Built-in self repair (BISR) will improve production quality. Improving yield and reliability, and decreasing test time, through excellent design tools

and test strategies will have a direct impact on costs and market potential for a range of high-volume applications.

In the sub-100-nm realm, smaller structures require new features to be integrated into the design flow. Effects have to be taken into account that could have been neglected in the past. New materials – such as those with low dielectric constant – require separate treatment.

TECHNODAT focuses specifically on physical problems that are symptoms of this fragility: noise transmission through substrate; power-supply noise; cross talk between interconnects; device-mismatch effects; and effects from α or neutronic radiation.

Activities are based on both modelling and measurement: the former helps predict and hopefully attenuate negative effects, while the latter contributes to tuning models. Modelling often has to switch from two-dimensional to new three-dimensional approaches. Definition of ad hoc test structures to monitor signal integrity is part of the project.

From prediction to correction

By combining experience, project partners intend to push chip design and manufacturing capabilities beyond their present levels to develop a competitive advantage for European companies in the sector.

Partners include chipmakers Infineon, Philips and STMicroelectronics, CAD and computer-aided engineering (CAE) enterprises CISC, Dolphin Integration, Hirex, IROC, ISD and Simplex, and the Fraunhofer, TIMA/INPG and University of Delft research institutes. Benefits of such a cross-disciplinary group include extensive cross-fertilisation of ideas.

Outcomes will benefit not only the partners but also the design community as a whole, through commercial offers from the six CAD/CAE partners, and scientific publications from the research institutes.

TECHNODAT aims to meet quantitative and qualitative challenges. At quantitative level, the project will help speed CAD. At qualitative level, new physical problems that are emerging at each technology generation may imply severe malfunctioning of the circuits. In particular, the project aims to predict physical problems so as to improve the resulting design. It also aims to detect errors as soon as possible to allow their correction.

All this will be achieved by:

1. **Accelerating** CAD through higher automation of the production/validation of basic blocks, involving multi-site development infrastructure for concurrent engineering;
2. **Predicting** physical problems through better knowledge of new deep submicron phenomena (noise transmission, cross-talk, radiation...) and acquisition of know-how to carry out physical modelling down to the 70-nm level;
3. **Improving** design robustness – some well-known actions are at the expense of circuit area or speed. TECHNODAT is helping decide when such safeguards are activated;
4. **Detecting** problems at design stage, after production or in the field, through efficient testing. Such methods defined at the design stage will increase reliability while reducing test cost and duration. BIST techniques will increase circuit reliability in the field; and
5. **Correcting** IC errors after production involves different techniques: T101 is focusing on BISR.

Improving technical edge

Starting points for further development often result from inter-company collaboration. This is true for many tools now in use within the European semiconductor industry. For example, more than 20 of the operational products and techniques standard at design centres of several of the project partners are a direct result of the earlier MEDEA A401 project.

For semiconductor partners, the MEDEA+ project is extending their know-how and capabilities in libraries and memory development, design and test activities, and silicon quality control. New methodologies and tools are being added to each company's design process to extend or replace existing solutions. In addition, valuable experience is being gained in working below 100 nm.

Project results are expected to include an improved compromise between standard cells and semi-custom, easier on-the-fly generation of hot cells and greater accuracy in meeting design constraints. Partners also anticipate achieving much-improved implementation of the techniques involved in standards-based, multi-site library development.

For the CAD companies, TECHNODAT will lead to new CAD and CAE tools to improve design and test methods used for developing commercial products. New ways of increasing yield, improving test techniques and reducing time-to-market will all help European companies improve their edge in highly competitive world markets.

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.