PROJECT PROFILE

T104: Safe IC design for robust applications (SIDRA)

ENABLING IC TECHNOLOGIES FOR APPLICATIONS

Partners:

ATMEL
ETH Zurich
Infineon Technologies
Philips Semiconductors
Robert Bosch
STMicroelectronics
Vienna University of Technology
X-FAB

Project leader:

Wolfgang Wilkening,
Robert Bosch

Key project dates:

Start: August 2004
End: September 2006

Countries involved:

Austria
Germany
Italy
The Netherlands
Switzerland

Robust operation of complex power and mixed analogue/digital devices in harsh environments is essential for the electronic systems deployed increasingly to monitor vital control and safety functions in modern motor vehicles. Similar reliability standards are necessary in many other applications, ranging from security to communications and even some consumer appliances. A particularly important requirement is to ensure that such components are resistant to damage caused by electrostatic discharge (ESD). The MEDEA+ T104 SIDRA project is responding to this need by developing simulation-guided design methods that for the first time will aim to address ESD protection at a whole-chip level.

High voltages and mixed signal applications make the latest chip designs increasingly difficult to protect against fast transient electrical pulses. An additional challenge comes from future technologies with the extremely thin gate oxide layers. Given the continuing trend to greater system-on-chip (SoC) integration, ESD robustness is increasingly a matter of the whole chip, rather than only the input/output interface cells. Consequently, the complete device — including package, substrate and core — must be taken into account.

The MEDEA+ T104 SIDRA project set out to develop and verify simulation-guided design methods that will eliminate weaknesses in integrated circuits (ICs) subject to fast transient pulses, so improving reliability. The new methods will reduce design cycle time and increase development productivity. The project consortium comprises many of Europe's leading chipmakers — Atmel, Bosch, Infineon, Philips, STMicroelectronics and mixed-signal foundry X-FAB — together with research institutes, universities and a software house, co-ordinated by Bosch.

Work is focusing on mixed-signal ICs such as those for car applications that — due to their safety-critical nature, the hostile operating environment and a high degree of heterogeneous complexity — are subject to extreme specifications. In addition, the project will investigate applications such as smart cards and platform security facing similar requirements.

Difficult challenges

ESD depends on where and how the static charge is accumulated and how its build-up is dissipated. Several industry-standard models define how chips should be tested for ESD sensitivity under different situations: the most important ones are the human body model (HBM) and the charged device model (CDM), which is becoming more and more important.

Both these models address non-powered ICs, whereas for systems the main hazard arises from system level ESD (Gun test). If powered devices are subject to transient electrical overstress, the main risk arises from transient latch-up (TLU). All these events may result in malfunction or even destruction.

The risks must be detected and excluded at the design stage to avoid first making and

characterising a chip, and then having to redesign it. Considerable progress was made in dealing with CDM at device level in the earlier MEDEA+ T102 ASDESE project. However, several issues arose beyond its scope; these are now being tackled in SIDRA.

As a significant new step, SIDRA expands from device- to chip-level ESD protection. Success in this respect will represent an extremely important breakthrough, giving a significant boost to the future competitiveness of the European semiconductor industry.

Common test structures

The first step is to define a common set of test structures that reflect the various failure mechanisms, while additional test structures containing technology- and product-specific components are designed individually by the partners.

HBM, CDM and Gun phenomena are being addressed. New characterisation methods for ultra-fast transmission line pulsing (TLP) are being developed and the effects of transient stress investigated. Failure analysis based on optical mapping is being developed for the detection of leakage currents caused by electrostatic discharges.

Device simulation is extending to complex computational applications covering several devices under ESD. New approaches for circuit simulation are modelling all relevant parts of complete ESD chip protection, including simplified core blocks and, where necessary, parasitic elements from sources such as the wiring, substrate and package.

The approach is to design and produce test structures and circuits in various technologies employed by the partners, and to evaluate these with new characterisation methods and simulation. The increasing sensitivity of devices in modern technologies makes ESD and, to some extent, TLU the leading causes for redesign, so the impact on time to market will be dramatic.

New guidelines

One of the most important results will be the definition of design guidelines guaranteeing sufficient ESD robustness for chips processed in current state-of-the-art technologies, such as sub-100 nm CMOS and advanced Smart power, including silicon on insulator (SOI). These will also enable the chipmaker partners to expand their existing knowledge of ESD-robust design into new types and generations of technology.

Consideration of system aspects during the design phase for automotive applications, which combine sensitive analogue functions with digital and power circuitry, will reduce development time by eliminating repetitive loops. The number of redesigns due to unacceptable transient pulse sensitivity of application-specific ICs should be reduced by about half as a result of the acquired knowledge.

In the final phase, partners will simulate agreed test structures processed in their individual technologies and validate the results against measurements. Possible deviation between simulations and measurements will be analysed, and any necessary additional characterisations and/or simulations performed in a second validation loop. Ultimately, the new methods and application case-studies will be documented and disseminated.

Broad benefits

Competitive advantages achieved through this project will help semiconductor partners to remain at the leading edge of the power-differentiated IC market. The results will enable the technology provider companies to offer top level design kits that take into account ESD and TLU effects, providing additional strong arguments to attract new customers.

Thanks to previous related projects — ASDESE and ESPRIT ESDEM — Europe is already strong in the ESD field. In order to consolidate its position, the consortium will present data from SIDRA as proposals to the relevant standardisation bodies dealing with CDM, system level ESD, TLP and TLU — including the International Engineering Consortium (IEC) via the German Commission for Electrical, Electronic & Information Technologies of DIN and VDE (DKE) and the Electrostatic Discharge Association (ESDA).

For university partners, close collaboration with industry is enriching the curricula and providing PhD students with experience of research in fields of real industrial relevance. In particular, simulation-based examples from the project will be incorporated into future education and training, ensuring availability of adequately trained engineers in Europe.

In addition, academic partners have opportunities to develop prototypes of measurement set-ups that can be tested by industry during the lifetime of the project. This offers an ideal basis for future commercialisation, which in the longer term could lead to the start-up of new businesses, bringing the prospect of additional employment.

MEDEA+

MEDEA+ Office
33, Avenue du Maine
Tour Maine-Montparnasse
PO Box 22
F-75755 Paris Cedex 15, France
Tel.: +33 1 40 64 45 60
Fax.: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

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