PROJECT PROFILE

T126: Building-up embedded memories (BLUEBERRIES)

ENABLING IC TECHNOLOGIES FOR APPLICATIONS

Partners:

CNRS Marseille
Freescale
Ecole Normale Supérieure de Cachan
Philips
STMicroelectronics
TNI-Valiosys
Uni Nancy
YogiTech

Project leader:

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Key project dates:

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Countries involved:

France
Italy
The Netherlands

Manufacturers anxious to attract and retain sophisticated customers are continually striving to improve key characteristics of information and communications products, such as bandwidth, functionality, speed of operation and battery life. To deliver such improvements, designers are turning to complete system-on-chip devices, with fully integrated memory. The objective of the MEDEA+ T126 BLUEBERRIES project is to develop new physical processes and design and validation methodologies, including CAD flows, for the design and production of embedded random access memory (RAM). The processes, tools and know-how developed could be pivotal in preventing the eclipse of European chipmakers by strong competition from the USA and Japan in the provision of embedded RAM.

Third-generation mobile phones are a triumph of integration. In a package maybe no larger than a pack of playing cards, they combine wireless communications with multimedia functionality and yet consume power frugally enough to go several days before their batteries need recharging. The same could be said of many of today's electronic products. At the heart of many of them are complete system-on-chip (SoC) devices – integrating multiple complex electronic subsystems, including one or more processors and megabytes of embedded random access memory (RAM) all integrated on a single chip. The emphasis placed on memory is due to the increasing amount of data included in electronic devices to make them more 'intelligent'.

Embedded versus stand-alone

Choosing embedded over stand-alone memory brings clear advantages in these products. It removes the need for connections between chips (the 'interconnect wall'). It allows designers the use of ultra-wide data buses as well as flexible array sizes and orientations. In these ways, embedding memory can increase speed of operation, reduce power consumption and, of course, increase compactness.

It is not surprising then, that market researchers expect rapid market growth. Estimates have suggested that, by 2005, the annual worldwide SoC market may approach €40 billion. Extrapolating from a steady increase over recent years, others have predicted that the area of SoC occupied by embedded memory will average around 70% by 2005.

What is surprising is that the processes of designing and of fabricating embedded memory are not greatly automated. So, while the range of memory variants that may be specified by a customer is broad, the designer is usually constrained by cost to use an off-the-shelf solution. This is a prime motivation for the MEDEA+ T126 BLUEBERRIES project. The partners share the conviction that designers should have the design-automation tools that would enable them to provide custom designs closely tailored to customer requirements without long lead times.

BLUEBERRIES is considering three memory families: static RAM (SRAM), dynamic RAM

(DRAM) and magnetoresistive RAM (MRAM). When embedding SRAMs in a SoC, the particular difficulty is that each new generation is more susceptible than the last to soft error rate. Robustness is therefore a concern.

DRAMs are a different story. Their greater complexity has been such an obstacle to the automation of designing embedded DRAM that the partners believe urgent action is required

While MRAM is less mature, it holds great promise if it can be fabricated economically. It has already been dubbed as 'universal memory', because a single large block of embedded MRAM could potentially replace all of the SRAM, DRAM and flash memory combined in many applications today, embedded or not. And the result would consume less power.

Forecasts have predicted an annual worldwide market of €40 billion for embedded and stand-alone MRAM. In 2002, BLUEBERRIES partner Freescale (subsidiary of Motorola) fabricated what is reputedly the first 1 MB MRAM. Competition is stiff. MRAM R&D is strongest in the USA. Not only does Freescale have a strong position, but also IBM together with Infineon and Honeywell. In Japan, a joint effort is already under way at NEC and Toshiba to develop low-power MRAM, while a national MRAM research programme run by the Ministry of Economy, Trade and Industry (METI) is under consideration.

Ambitious programme

In choosing to consider SRAM, DRAM and MRAM in parallel, BLUEBERRIES' research programme is ambitious. The partners planned their work around the main process and design steps so as to maximize cross-fertilization between the different technologies. They aim thereby to develop advanced physical processes, architectures, design and validation techniques and tools, SoC requirements and demonstrators, and computer-aided flows for design and production of embedded memories of all three types.

They are also endeavouring to increase the range of embedded-memory solutions available, allowing customers and designers to trade off speed against power consumption according to their needs. However, making tangible improvements in density and yield to reduce the cost of embedded memories, without compromising robustness, is not easy in the face of concomitant increase in error sensitivity.

But the biggest challenge of all is demonstrating the feasibility of MRAM. An MRAM cell depends on a magnetic tunnel junction for its ability to store a bit of information. But under- or over-oxidation of the insulating layer can occur in existing fabrication processes. BLUEBERRIES is investigating an alternative technique using atomic layer epitaxy.

At the process level, the partners are investigating, among other things, novel DRAM configurations to accommodate smaller capacitor size and minimum capacitance reduction. As regards memory architecture, they are concentrating on increasing feature density, reducing time-to-market by reducing burn-in time, minimising power consumption, providing interfaces for many operating modes, modelling memory for performance analysis, and developing a new fault injector to help improve fault protection. Design verification is a further focus.

At the level of the SoC, an application, such as a 3G mobile phone, is being modelled to improve the partners' detailed understanding of memory requirements for typical SoC applications. Chipmakers STMicroelectronics, Freescale and Philips are carrying out SoC integration on silicon for different types of memory but with a preference for MRAM down to 65nm.

Deliverables include SoC demonstrators: a macro cell and a test chip (a functional structure proved on silicon) for each combination of memory family (SRAM, DRAM, MRAM) and generation (90 nm, 65 nm). Two additional test chips – a 90-nm one and a 65-nm one – will each incorporate embedded SRAM, DRAM and MRAM.

Satisfying customers precisely

BLUEBERRIES will directly boost the competitiveness of European companies in several markets, notably those for SoCs and electronic-design automation tools. It will also improve and consolidate the know-how of all of its partners in their respective spheres of expertise. They expect to emerge much better equipped to design embedded memories of different types to satisfy the requirements of their customers more precisely than they can at present.

For STMicroelectronics, Philips and Freescale, the three global BLUEBERRIES partners in silicon design and fabrication, this forward leap will complement the large investments in their joint Crolles-2 R&D facility in France. It will also catalyse the creation of new jobs in Europe, since many European companies in the supply chains for microelectronic products will benefit from better embedded RAMs and SoCs.

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