PROJECT PROFILE

T201: CMOS logic 0.1 μm and below

IC TECHNOLOGY INTEGRATION

Partners:

Air Liquide
Aixtron
Bull
IMEC
Inorgtech
INPG/CNRS
Jobin Yvon
Leica Microsystem Lithography
LETI
LTM/CNRS
Philips
STMicroelectronics

Project leader:

Guillermo Bomchil,
STMicroelectronics

Key project dates:

Start: January 2001
End: December 2002

Countries involved:

Belgium
France
Germany
UK

Transistor downsizing is proceeding faster than originally forecast in the International Technology Roadmap for Semiconductors (ITRS). Production of integrated circuits with 100-nm feature size will start in 2003, and the 65-nm node will arrive sooner than previously predicted for 2005. Various new materials and process technologies are currently under investigation, but no clear consensus has yet emerged on precisely how the coming chip generations will be manufactured. The consortium involved in MEDEA+ project T201 aims to equip Europe's semiconductor industry with the tools and techniques needed in this area to maintain a leading position in the world marketplace.

Today, CMOS process technology with 130-nm printed feature sizes is in production. Although it has been possible since 1999 to produce gates with physical details of 100 nm in nominal 150-nm geometries, true 100-nm technology has yet to arrive. A primary objective of MEDEA+ project T201 is therefore to achieve full 100-nm integration, and to prove this by designing a very powerful demonstrator chip that will be manufactured in 2003.

In addition, the consortium of 12 highly qualified partners from five European countries will co-operate in the development of advanced gate modules incorporating high-k dielectrics for devices of the next technology nodes at 65 nm and below. Using an innovative metal organic chemical vapour deposition (MOCVD) system, for the deposition of new materials, the gate module will initially be characterised by being embedded in a core process.

The timely integration of 100-nm CMOS in line with the roadmap of major semiconductor manufacturers will have a highly positive impact on the business prospects for the European participants Philips and STMicroelectronics, with associated benefits in terms of direct and indirect employment.

Pursuing alternative approaches

Because appropriate optical lithography for gate and contact hole patterning was not available early enough, the team is proceeding with a 'mix and match' approach devised by STMicroelectronics and Leica, which combines e-beam direct writing and optical lithography. It might prove also to be a very useful approach for ASIC manufacturers.

Research partner IMEC is nevertheless pursuing a fully optical solution implementing 193-nm lithography for the critical levels. Employing some of the latest photoresist materials, it has demonstrated the feasibility of printing 100-nm lines and spaces – as well as isolated 70-nm lines – by using optimised illumination conditions in conjunction with advanced resolution enhancement techniques.

Systems manufacturer Bull will design a demonstrator incorporating RAM and ROM memory as well as 3000 standard cells, which have to be adapted to the new process conditions. Comprising more than 54 million transistors, 300 million contacts/vias and some 9 km of interconnections, the demonstrator will be based on a central processing unit (CPU) already being made

by STMicroelectronics in 180-nm geometry. However, the goal is to reduce the cycle time from the present 7.5 ns to 5 ns – for which 120-nm technology is mandatory. This exercise constitutes an essential step in opening the road to volume production of the new chips by the semiconductor fabricators.

Open questions

For the high-k dielectrics/gate module, open questions remain concerning industry's choice of both the preferred material and the deposition technique. Although the project's use of an MOCVD-based cluster tool developed by Aixtron for integrated processing has great competitive potential, other options do exist.

Many different binary and or ternary compounds are potential candidates for the dielectric. Probably only one of these will come into general use, as the global scale of the economy imposes a de facto world standard.

Several partners are collaborating in the evaluation of novel gas-phase precursors for use in CVD, and in the development of a precursor injection unit that allows a very precise flash evaporation of barium, strontium and the rare earth-elements, for which there are no stable precursors in standard MOCVD. Strontium/titanium oxide ($SrTiO_3$), which can now be deposited in the form of smooth and uniform crystalline films, has emerged as an early favourite. INPG/CNRS is contributing to an effort to define parameters and select chemical systems for reliable application at temperatures below 500°C.

Aixtron and instrument manufacturer Jobin Yvon are co-operating in the provision of in-line metrology for accurate control of the process. Determination of the environmental, health and safety consequences of employing new materials is another important aspect of the investigation, for which STMicroelectronics has initiated a special action.

A number of approaches also exist for the metal contact. Initially, standard titanium nitride is being tested as the barrier material with tungsten to fill the contact hole. The deposition of platinum and ruthenium by MOCVD in the cluster tool will also be explored. The latter material, in particular, is receiving increasing attention from the IC makers because of its easy process compatibility.

STMicroelectronics and LETI at Crolles and Philips and IMEC at Leuven are working on complementary approaches concerning the 100-nm process modules. The most promising options will be optimised during the integration phase in the Crolles manufacturing facilities.

Across-the-board benefits

At a first stage, Philips Semiconductors and STMicroelectronics will jointly implement the technology on a new 300-mm pilot line in construction at STMicroelectronics' Crolles plant. Subsequently, it will be transferred to additional production sites of the two companies, allowing rapid incorporation of 100-nm capabilities into their product strategies. As with earlier projects, worldwide customer requests for prototypes should quickly lead to a full validation phase, followed by industrial exploitation.

The industrial equipment and materials supplying partners will exploit the results in their own specific domains of action: Aixtron for the MOCVD equipment, Inorgtech for the precursors and Air Liquide for the required gases and chemicals.

For Leica, MEDEA+ project T201 provides an opportunity to demonstrate the strengths of e-beam direct writing associated with optical lithography. The mix and match approach is considered a useful means of push down resolution in advance of the availability of industrial optical scanners. In fact, it could even become a preferred strategy for prototyping by manufacturers of ASICs (application-specific integrated circuits).

Although research institutes and universities do not themselves exploit the project results, the experience gained constitutes an important element in their scientific/technical programmes. For IMEC and LETI, participation in T201 reinforces their strategy of strong co-operation with major IC and equipment suppliers working on key technologies for the IC industry. In particular, bilateral agreements announced early in 2000 between Philips and IMEC and between STMicroelectronics and LETI are ensuring full-time involvement of these institutes in leading-edge industrial research.

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