PROJECT PROFILE

T207: 65nm CMOS process in 300mm wafers (65nm CMOS300)

IC TECHNOLOGY INTEGRATION

Partners:

Air Liquide
Aixtron
ASMI
Bull
CEA-LETI
CNRS-LMGP
CNRS-LTM
Epichem
Fraunhofer Institute
HORIBA/Jobin-Yvon
IMEC
Jipelec
Lamers High Tech Systems
Leica Microsystems Lithography
Motorola
Philips Research
Philips Semiconductors
STMicroelectronics
Trikon
University of Savoie

Project leader:

Guillermo Bomchil,
STMicroelectronics

Key project dates:

Start: January 2003
End: December 2005

Countries involved:

Belgium
France
Germany
The Netherlands
United Kingdom

The goal of the MEDEA+ 65nm CMOS300 project is to develop and integrate a full 65nm node CMOS logic process in a 300mm diameter wafer manufacturing facility by 2005, ahead of the global technology roadmap. A further objective is the design and manufacture of a demonstrator conforming to 65nm design rules. Optimisation and implementation of enabling techniques in the CMOS process to achieve these specifications on 300mm industrial equipment will enable European chip and equipment manufacturers to substantially increase worldwide competitiveness. The project is also enabling members of the consortium to collaborate in the common goal of assembling the best competences available in Europe.

The MEDEA+ T207 65nm CMOS300 project is intended to result in the achievement of 65nm node CMOS manufacturing capabilities on 300mm wafers in Europe by 2005. This would be ahead of the time frame predicted in the 2002 update of the International Technology Roadmap for Semiconductors (ITRS). For the first time, European players would be among the few companies worldwide able to use the most advanced CMOS logic technologies for chipmaking.

Manufacturability in 300mm wafers and process-related industrial aspects are receiving the highest attention throughout the project. The goal is to ensure the rapid transfer of results into industrial exploitation by chipmakers and to have a direct impact on European equipment suppliers contributing to the project – including those in optical lithography, electron beam lithography, high and low k dielectric materials, characterisation and test techniques.

Exploiting earlier research

To achieve these goals, the 65nm CMOS300 project is using exploratory and generic work performed in previous or current European projects – including MEDEA+ projects T201 CMOS logic 0.1 μm, T301 0.1 μm Fab, T302 ALADIN+, T303 CLASS and T401 FLUOR, as well as the European Commission Information Society Technologies (IST) ACTION, ARTEMIS, NESTOR and ULISSE projects – and implementing the most promising solutions in process modules using industrial 300 mm equipment sets.

Optical lithography is being used for module development and full CMOS process integration. It is expected that the final assembly will benefit from rapid progress in 193nm optical lithography. The use of 157nm optical lithography could be also introduced in a manufacturing environment by the end of the project, following a first assessment at the R&D laboratory level. In parallel, e-beam direct write technology is being fully exploited for early module development and advanced prototyping.

Front-end process modules are being scaled or new ones developed – the choice of modules depends on maturity for industrial use. Device architecture is also being optimised to maximise performance and minimise leakages in line with envisaged applications. Back-end processes are targeting a double damascene multilevel metallisation copper/low k dielectric architecture. Integration

choices are being assessed by test structures and also by processing a complex demonstrator, including embedded SRAM.

Mobilising European strengths

The dramatic technological acceleration in the ITRS will result in the development of high-complexity products, such as full system-on-chip (SoC) devices, associated with increased performance, higher technical complexity and necessary decreases in cost per function. In addition, new challenges are being created by the introduction of 300mm wafers in manufacturing.

T207 brings together most of the European excellence in microelectronics. In addition to the three industrial partners, it involves the leading technological research institutes, internationally recognised academic teams and highly competitive equipment suppliers – including SMEs.

Without this MEDEA+ programme for the 65nm node in Europe, it would be impossible to mobilise the power that is required for getting the key players in the European market to work together towards the goal of achieving a European-developed technology that is competitive worldwide. One single company would not be able to achieve this ambitious goal alone. Through this strategic project, Europe has the possibility of meeting the needs of worldwide business and establishing firm leadership in a key enabling technology that can be useful for all information, communications and entertainment applications.

The ITRS roadmap presents an industry-wide consensus on the best current estimate of the industry's research and development needs over the next 15 years. It is the result of worldwide consensus building and has been used extensively to benchmark the goals of the MEDEA+ 65nm CMOS300 project – comparing planned activities and quantitative targets with the ITRS recommendations and predictions.

Leading semiconductor manufacturers worldwide, including members of this project consortium, are already manufacturing products with 130nm technology node specifications. The next technology node is 90nm, which is expected to enter into volume industrial production in 2004.

Motorola, Philips and STMicroelectronics (Crolles 2 Alliance) already have a jointly developed CMOS 90nm node. In addition, there is a technology agreement with TMSC. All partners agreed on common design rules and generic core process.

The 90nm technology developed was validated on fully functional test chips produced first on the STMicroelectronics/ Philips pilot line in Crolles, France and at TSMC's R&D facilities in Hsinchu, Taiwan by the end of 2001. The process was transferred and validated in the Alliance Crolles 2 line early in 2003. First test chips included 1- and 4-Mbit embedded SRAM functions.

The SRAM density of 735 kbit/mm^2 achieved was among the highest in the industry. The partners increased the density further, reducing the SRAM cell size from its initial 1.36 microns to 1.00 microns square area.

All these announced results indicate that 90nm node CMOS technology is already well established and is entering into a phase of prototyping that will be followed up by volume production.

Maintaining a strong position

Information published by Dataquest shows that the three major European semiconductor manufacturers are among the top ten worldwide. World leader Intel however has revenues three times bigger than the one ranked number two, and the rather small differences between the remaining companies in the top ten show how important it is to come up with the right technology at the right time in the fiercely competitive environment of IC manufacturing. That is why the MEDEA+ 65 nm CMOS300 project is so important to the competitive power of the European microelectronics industry!

As Motorola, STMicroelectronics, Philips and now operate their 300mm line in Crolles, a significant increase of employment is expected, not to mention the number of indirect jobs generated by the site. This project will also contribute to new business development because the equipment and material project partners will expand their opportunities for innovative applications in the silicon industry. The project is expected to strengthen the position of equipment suppliers and further expand their product portfolios for mainstream silicon industry applications.

For the research institutes and academic teams, the validation of advanced concepts and modules on the industrial line in Crolles represents a valuable means of extending their influence and attracting interest from other industrial partners for future joint development programmes.

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.