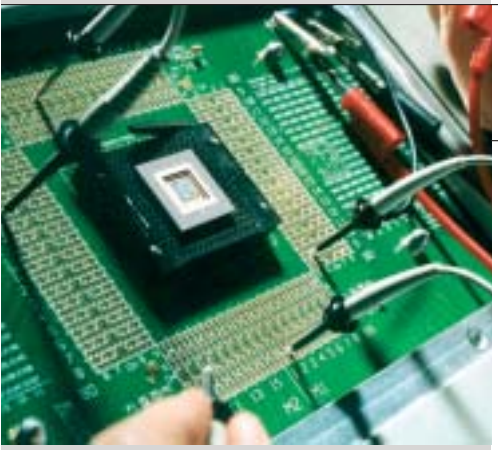
PROJECT RESULT

Design methodologies



A503: Advanced Solutions for SoC innovative testing in Europe (ASSOCIATE)

Reducing testing costs for complex circuits

Testing can easily account for 35% of the total cost of a complex chip. The growing popularity of complete mixed-signal systems-on-chip using multiple embedded intellectual-property cores means the figure is set to grow. To turn the tables on this trend, the MEDEA+ A503 ASSOCIATE project has developed design-for-test (DfT) and design-for-debugging (DfD) tools and techniques, and forged from them a structured testing methodology. With one DfD product already on the market as a result, it provides a shot in the arm for the automatic testing industry in Europe against strong competition from the USA.

The functional complexity required of modern chips places heavy demands on the design process. Eager to minimise costs and speed time to market, manufacturers have moved towards reuse of circuit modules. Where possible, circuit functions are realised not by designing new circuits from scratch but by reusing ready-designed circuit modules exploiting the complexity of 'intellectual property' (IP) cores. Taking full advantage of IP-based design requires new test techniques and integration of test resources in the circuit.

Test cost spirals

Testing complete system-on-chip (SoC) devices is time consuming and expensive – such chips can contain up to 250 million transistors. Test access to the many embedded cores can be physically difficult to achieve given the limited chip pin count. A conservative estimate from the Semiconductor International Association (SIA) reckons 35% of the total cost for a SoC goes on testing. And the situation is getting worse. In the1999 edition of the International Technology Roadmap for Semiconductors, it was predicted that if the trend continued unchecked, the cost per transistor of testing complex chips would exceed that of manufacturing them within 15 years.

In the MEDEA+ A503 ASSOCIATE project, European players from all stages of the product production cycle joined forces to push back the boundaries of testing. They worked on three areas:

1. Design for test (DfT), in which structured provision for the testing of a chip is made while it is being designed;
2. Design for debugging (DfD), a novel approach in which features are incorporated into a SoC design to enable the rapid identification of any design flaw or processing fault that causes a device to fail during test; and
3. Improving the efficiency of test applications and integrating DfT and DfD tools into the larger design process.

From testing to debugging

In its work on DfT, the MEDEA+ consortium had notable success in developing built-in self-test (BIST) structures for logic, memory, analogue and mixed-signal blocks. Added to the design of an embedded core, BIST structures generate and apply test patterns to their core, and then evaluate the response. ASSOCIATE's achievements include, among others, an at-speed memory BIST for detecting delay faults and a low-power BIST technique that can reduce switching activity during scan shifting,

cutting power consumption during test by up to 40%.

ASSOCIATE's approach to DfD involves embedding instruments inside SoCs. Running on an external controller or personal computer, software counterparts separately created by the partners communicate with these instruments over an IEEE-standard test access port. In this way, the cause of test failures can be traced.

The partners also devised a description language and software controller that enables hardware for breakpoint insertion and control to be automatically generated from a high-level specification (effectively independent of the device being developed). With this feature added to a logic core embedded in a SoC, a debugger can make a controlled stop in the normal operation of the core, change its state and resume operation – an invaluable debugging aid.

Thanks in part to the project's advances in DfD, Temento Systems – a partner that provides software tools for electronic test automation – has been able to develop a new product, DiaLite Instrumentation (DLI), now commercially available. It supports designs in hardware description languages such as very high-speed integrated circuit (VHDL) and Verilog as well as designs that combine elements of both.

Improving test efficiency

Among the contributions that the MEDEA+ project has made to improve test-application efficiency is a high-level description language and corresponding software for translating test programs from one format into another. Porting mixed-signal designs by hand can take weeks or months; now it can be done in a matter of days.

Using another new technique, the integral non-linearity of an analogue-to-digital converter (ADC) core can be estimated in a fraction of the time usually needed, by reducing the number of samples required. For a 12-bit ADC, for example, 8,000 samples now suffice for a task that used to require a million or more.

The main achievement of the project, however, has been to integrate DfT and DfD tools into a structured methodology from which many of the partners will directly benefit in their day-to-day operations.

EDA roadmap inspiration

The seed for ASSOCIATE was sown by the MEDEA+ roadmap for electronic design automation. Consortium members LIRMM and INESC contributed to a special chapter in the roadmap on testing. The serious and growing gap identified between the complexity of chips and their amenability to efficient testing encouraged the launch of ASSOCIATE. The partners promoted the roadmap internally and have stayed in touch with its co-ordinators throughout the life of the project, continually feeding back their findings.

Collaboration between ASSOCIATE consortium members was strong. They worked well together as a project team, but also established opportunities for intense and fruitful co-operation in smaller subgroupings. Infineon and LIRMM, for example, worked closely together on memory and low-power BISTs. Alcatel worked with Philips on debugging. And INESC transferred low-power BIST technology to TECMIC.

Not content to sit on their laurels, the consortium members together with new partners have already proposed a new MEDEA+ project on chip testing.

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Partners

Alcatel
AMI Semiconductor
INESC
Infineon
Italtel (in 2002 and 2003)
LIRMM
Philips Semiconductors
Tecmic
Temento

Project leader

Edgard Laes,
AMI Semiconductor

Key project dates

Start: July 2001
End: June 2004

Countries involved

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France
Italy
The Netherlands
Portugal

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