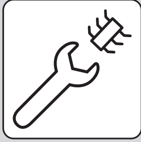
PROJECT RESULT



Enabling
IC technologies
for applications

T101: Technology-driven design and test for system innovation on silicon (TechnoDaT)

Design and test solutions deliver robust on-chip memories

The evolution of chip technology towards higher gate densities and new materials is resulting in additional constraints to be taken into account at the design level. Appropriate technology-dependent environments are necessary not only to accelerate or secure today's designs, but also to make future designs more readily feasible and testable. The TechnoDaT project addressed the challenges of acquiring new knowledge and determining how to handle soaring volumes of data. Its results are helping designers and test teams to extract maximum benefit from new technologies, without facing heavy overload.

Memory will take up to 70% of the silicon area on future system-on-chip (SoC) devices. Improving yield and reliability in this area, while decreasing test time, will have a direct impact on costs and market growth of high volume applications such as mobile communications, Internet and automotive systems.

Confronted with shared difficulties at deep submicron design level, Europe's three main chipmakers – Infineon, Philips and STMicroelectronics – pooled resources. They linked with five computer-aided design (CAD) companies and two research institutes in the MEDEA+ T101 TechnoDaT project.

This collaboration was a way to enable the CAD vendors to raise their design environments to a best-in-class standard, while the institutes would bring their expertise to bear on tuning and exercising low-cost test methods, enabling chipmakers to have early access to tools for advanced applications.

Time/cost problems overcome

The first problem was handling an increasing volume of design data without jeopardising quality. Three generations of CMOS logic were addressed: 130, 90 and 65 nm. For these, each new library of cells that is defined requires around 700 cells to be submitted to 100 tests. TechnoDaT helped eliminate this bottleneck by employing very efficient algorithms to activate the generation and validation of cells.

For logic cells, management of parallel computations reduced elapsed time to just a tenth of its former level. Now, a month can be saved in the design and qualification of random-access (RAM) and read-only (ROM) memories. Input/output cells can be characterised ten times faster. And a productive design flow for 65 nm CMOS libraries is ready, with a production cycle time divided by four.

The second area targeted cost-of-testing. Ever-increasing chip complexity creates growing requirements for automated testing, one of the most expensive processes in a fab. To counteract rising costs, TechnoDaT produced several efficient low-cost test solutions. Its on-board self-test system is ten times faster than commercial automated test equipment (ATE). A test simulation flow to debug test programmes before processing silicon proved able to shorten time-to-market by several weeks; and a 1:100 data compression technique minimises test duration in the fab.

A virtuous loop

A third set of problems came from the increasing fragility of devices due to progressive miniaturisation. The approach in the MEDEA+ TechnoDaT project was first to

model, then to predict undesirable effects, and finally to increase the robustness as soon as possible during the design process. Test chips helped close this virtuous loop with model tuning based on silicon measurements.

Cross-talk and voltage drops can seriously affect timings and signal integrity in 90 and 65 nm circuits. Different levels of design abstraction were linked to form a consistent verification flow, which can now be commercialised. To preserve accuracy, each technology generation also requires more sophisticated models: for example, TechnoDaT had to include coupling capacitances for 130 nm, 3D effects for 90 nm and inductive effects for 65 nm.

Process variations are a cause of poor yield – increasingly so with the move from 90 to 65 nm design rules. To secure the design of analogue and mixed-signal applications, a tool was developed to assess the quality of sub-100 nm CMOS simulation models. Without proper actions, the higher density of logic gates on a chip would increase the sensitivity to natural radiation. The TechnoDaT equipment permits accurate evaluation of these effects in a reasonable time, while a new simulator runs 100 times faster. In parallel, novel design techniques alleviate the effects of field failures for memories. Substrate noise is another physical phenomenon against which TechnoDaT provides simple but efficient improvements.

Investigating limits

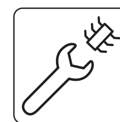
Libraries of proven test structures for 130 and 90 nm nodes made it possible to investigate the limits of technology, bearing in mind constraints such as power consumption. This resulted in design guidelines re-usable for future technologies.

In addition to digital CMOS, the consortium worked on analogue CMOS, BiCMOS and non-volatile memories – technologies widely used in equipment such as mobile phones. To benefit from CMOS for mixed-signal SoCs, it is important to avoid expensive analogue technology add-ons. For this purpose, a reliable mixed-signal design database was set-up to prevent problems during production ramp-up.

Some 60 papers were published and 20 patents filed. Project innovations included two yield-enhancing world firsts: a combination of diagnosis and self-repair for memories; and on-chip analogue signal generation for built-in self-testing of mixed-signal circuits.

The SoC approach places stringent demands on core design, for which this project provided an effective test platform. Furthermore, the industrial partners adopted common standards – open library architecture (OLA), core test language (CTL) and standard test interface language (STIL) – to facilitate interoperability and data exchange. This accelerated availability of co-operative results such as the Philips/STMicroelectronics library for 90 nm CMOS.

TechnoDaT's results will enable designers to use new technologies to achieve high quality with reasonable design times and at affordable cost. This investment is already being exploited on existing technologies by the project partners; the tools, flows and test-boards will remain valid for coming generations. In addition, ten new CAD design solutions will be marketed by the participating SMEs.



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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon for the e-economy.