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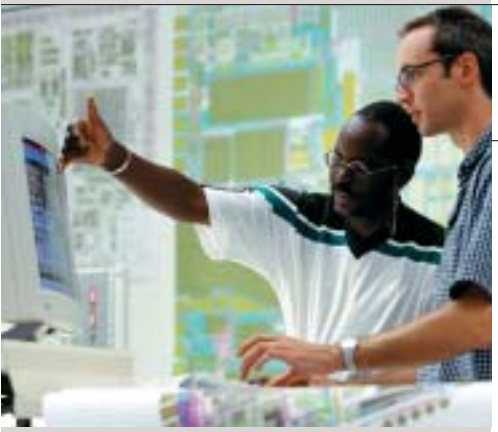

T102: Application Specific Design for ESD and Substrate Effects (ASDESE)

Design tools increase immunity of chips to electrostatic discharge and substrate noise

Electrostatic discharge (ESD) is a chip killer, both during fabrication and in their working lives.
And the problem is growing as the reduced dimensions of next-generation chips make them all the more vulnerable to ESD. The MEDEA+ T102 ASDESE project has now developed powerful simulation methods that enable ESD susceptibility to be reduced during initial design. The project also elaborated simulations for substrate-borne noise that provide a better understanding of how a chip performs and how its design can be optimised.
The result will be fewer costly redesigns and less failures in the field.

Semiconductor manufacturers are keenly aware that modern electronic systems depend on robust chip design. But as feature sizes reduce ever further, electrostatic discharge (ESD) is an increasing source of concern as unreliable chips can lead to serious liabilities, particularly in safety-critical applications such as automotive electronics or in data failure on smart cards. The impact can be enormous – not only directly in the application itself but also in public acceptance. Chipmakers observe there has been a doubling over the past few years of specifications that include detailed ESD characterisations.

Since the level of integration continues to grow, gate oxides are becoming thinner and junctions shallower. Chips are more vulnerable to overvoltage, the voltage design window is getting smaller, and it becomes more difficult to protect against ESD. A chip design that does not fully take into account ESD and substrate-borne noise is more likely to fail. Chipmakers have to go through a redesign cycle, if the first iteration proves to be unreliable – and each new iteration costs hundreds of thousands of euro in addition to the time delay.

The MEDEA+ T102 ASDESE project therefore set out to develop simulation-guided design methods to assure ESD robustness and prevent undesirable substrate coupling effects. The project was initiated by Bosch, which had previously been involved in ESD protection design. Bosch experienced that integrating modelling into the design methodology will offer a lot of advantages with respect to more robust circuitry. But it also realised that a single company alone would not be able to develop the necessary design methods. Therefore a consortium of interested parties was formed, with complementary abilities in design areas. Members included chipmakers, universities, software houses and small and medium-sized enterprises (SMEs).

Showing the whole picture

Conventional stress models for ESD do not show the full picture. The widely used Human Body Model (HBM) envisages ESD from contact with a human body and has a duration of more than 100 ns. This is because the human body is a relatively poor conductor with a relatively long resistive-capacitive time constant. The Charge Device Model (CDM) simulations developed by ASDESE can handle discharges of as short as 1 to 2 ns, with currents five times higher than the conventional HBM model.

ASDESE developed a spark-free CDM tester characterisation method; it is not acceptable to use electrical sparks to characterise

the ESD behaviour of chips, because they compromise repeatability. In addition, the project exploits optical methods applied to the underside of the chip – the substrate – to measure temperature and charge density close to the regions where ESD stress occurs. These measurements are then fed back into the circuit models, so that it may be further refined.

The MEDEA+ project has validated device models for CDM. Chip manufacturers within the consortium fabricated special test structures using their own specific manufacturing processes and device technologies. CDM simulations were applied at the design stage, and the resulting chips thoroughly tested. The results indicated that the required level of immunity had been achieved and that CDM subcircuit models worked well. In the meantime, the design guidelines that have been deduced are now being used in everyday chip design.

Integrated design environment

A different approach was used to tackle the various undesirable substrate effects, where crosstalk and noise may be coupled from one part of the circuit to another via the silicon substrate. Although methods for eliminating these effects already existed, ASDESE developed an integrated design environment that could handle much higher complexity.

One of the major achievements of the substrate work was the controlled design of a transimpedence amplifier chip that operates at 30 Gbit/s. This is a very high operating frequency, and the success of the design is due to the substrate simulation that enables these various effects to be controlled.

Strength in the consortium

The consortium achieved impressive results. It was not feasible for a single member to carry out all the research, neither in terms of work nor in terms of expertise. These are specialised areas and there are only a handful of experts working on the various topics in each company. The overall atmosphere was highly supportive, and project meetings especially fruitful – they provided a forum for discussing experiences and problems, and for each partner to enhance their own competences.

In global terms, the value of ASDESE cannot be underestimated. The partners have issued design guidelines for ESD robust design and for the simulation-guided control of substrate coupling. The results of their work have been widely disseminated through papers and contributions to key international conferences. A public workshop was also held at the 2002 European Solid-State Device Research Conference (ESSDERC) in Florence (Italy).

The outcomes of this MEDEA+ project have placed Europe at the forefront of solutions for these design problems, which in turn will support the development of even higher levels of integration. European chipmakers will be able to speed time to market with reduced chip redesign, and field failures will be reduced. The reputation of European chip manufactures for reliability will continue, and will help them to maintain an increase of their global market share.

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Partners

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Cadence Design Systems
IMEC
Infineon Technologies
Philips Semiconductors
Robert Bosch
STMicroelectronics
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Key project dates

Start: April 2001
End: June 2003

Countries involved

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